Recycling GaN for vertical power device performance

Researchers see potential cost savings for key electric vehicle markets.

MIRISE Technologies Corp, Nagoya University and Hamamatsu Photonics K.K. in Japan have reported on the potential for recycling gallium nitride (GaN) substrates with a view to reducing costs for high-performance power devices [Takashi Ishida et al, Appl. Phys. Express, v17, p026501, 2024]. The team comments: "The proposed recycling process is an effective method for reducing the cost of GaN substrates and has the potential to encourage the popularization of GaN vertical power devices."

Vertical devices presented up to now tend to be produced on expensive freestanding or bulk GaN substrates. Lateral devices can be produced on lower-cost substrates, like silicon, particularly for the lower voltage ratings.

Previous work has investigated the electrical performance of lateral GaN high-electron-mobility transistors (HEMTs) on GaN substrate before and after the laser slicing process that is used to reclaim the expensive GaN substrate. A thick epitaxial layer was added to the reclaimed wafer after slicing, but the electrical properties of devices fabricated on such recycled wafers has not been reported previously.

The potential of GaN as a premium material for power electronics is based on a high critical field (~10x that of silicon) and high channel mobilities (~2x those achieved in devices on silicon carbide, SiC). Another advantage of GaN over SiC is a lower epitaxial growth temperature, which reduces production cost.

MIRISE was founded in 2020 to carry out "research and development of in-vehicle semiconductors and development of electrical components that use semiconductors". The company is jointly owned by DENSO Corp (51%) and Toyota Motor Corp (49%). Hamamatsu Photonics produces optical sensors, light sources, and systems that use these components.

The researchers see high potential for vertical power devices in "high-power applications such as in-vehicle inverters that control main motors".

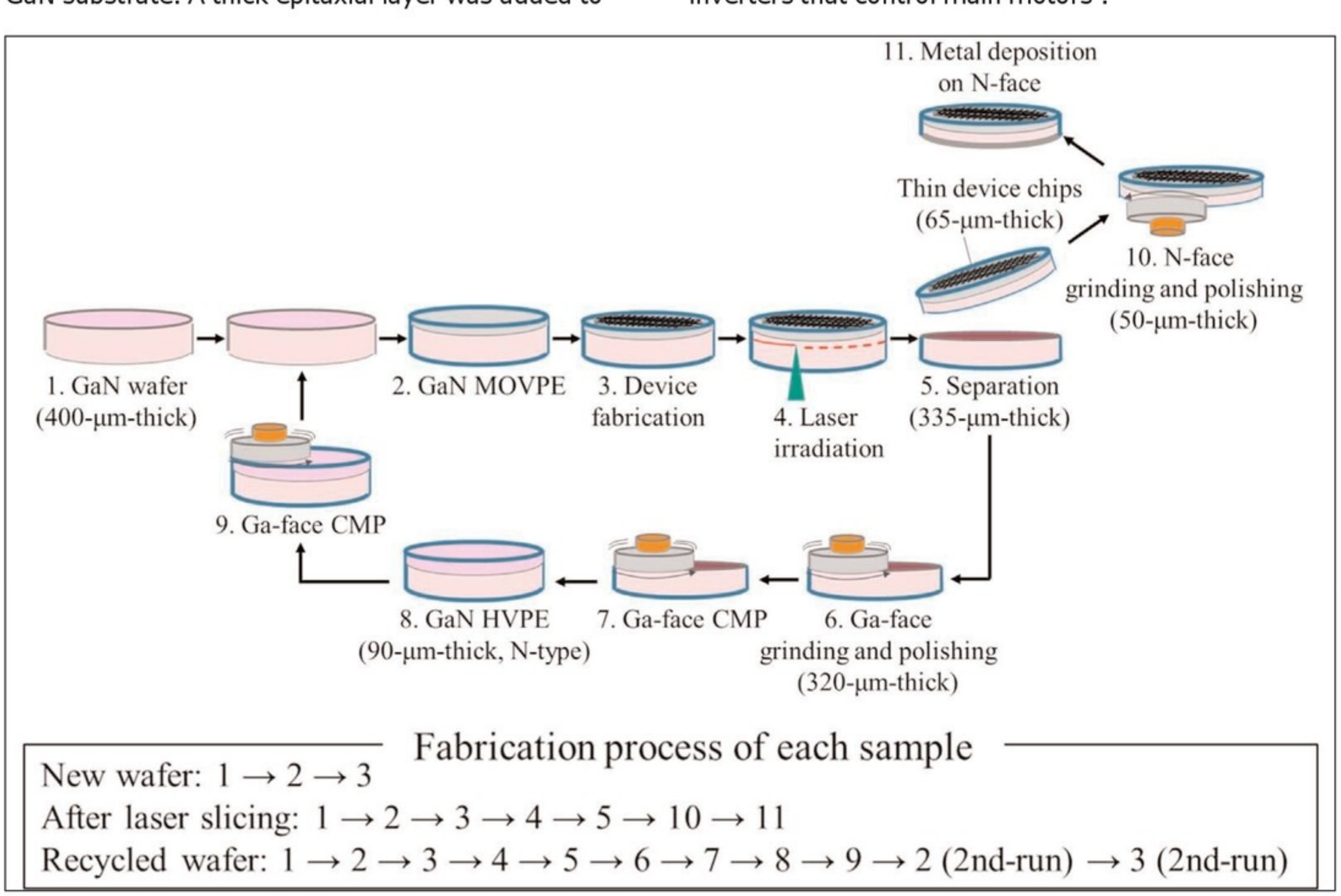

Figure 1. Overview of GaN substrate recycling through laser slicing.

The recycling consisted of separating a relatively thin layer with fabricated devices from the bulk of the GaN substrate (Figure 1).

The separation was accomplished using a 532nm focused laser beam from the N-side (bottom) of the wafer. The GaN decomposed into Ga metal and N gas at the focal plane in a two-photon absorption process. The focal plane could be adjusted to give different thicknesses for the separated wafer.

After the separation the rough separation surfaces were smoothed by grinding and polishing before further processing.

For the device wafer, processing was completed with deposition of the N-side metal and assembly into packages. The recycled wafer was subjected to chemical mechanical polishing (CMP) and hydride vapor phase epitaxy (HVPE) to return it to a state ready for further metal-organic vapor phase epitaxy (MOVPE) and fabrication.

The researchers comment: "It is indispensable to avoid wafer cracks for the success of the recycling process. To avoid wafer cracks, the suppression of the wafer warp caused by thinning wafer thickness is necessary. In particular, the amount of Ga-face grinding and polishing after separation should be minimized."

The researchers fabricated lateral metal-oxide-semiconductor field-effect transistors (MOSFETs) and vertical PN diodes.

The MOVPE device layers consisted of 4μm n^--GaN drift layer and 2μm p-GaN on n^+-GaN substrate. The n^-- and p-doping concentrations were 1x and $5x10^{17}/cm^3$, respectively.

The n-type MOSFET source and drain regions were fabricated using Si ion implantation through windows in the 100nm silicon dioxide (SiO_2) capping layer. The n-implant and p-body dopants were activated by 1050°C annealing in nitrogen for 5 minutes.

PN diodes were fabricated by removing the SiO_2 layer and creating beveled mesa structures for edge termination. The bevel angle and depth were 6° and 30μm, respectively.

The MOSFET gate insulation was provided by 100nm SiO_2 from plasma chemical vapor deposition (CVD). The MOSFET gate, source, drain and body electrodes were 160nm sputtered nickel (Ni).

This nickel deposition also provided the anode terminal on the p-side of the vertical PN diodes fabricated on the same wafer as the MOSFETs. The n-side cathode consisted of 500nm sputtered aluminium (Al) on the backside of the wafer.

Key characteristics for the MOSFETs for devices fabricated on fresh wafers showed somewhat better average performance after separation (Figure 2). However, the vertical PN diode structure did suffer some slight degradation in leakage under reverse bias after separation.

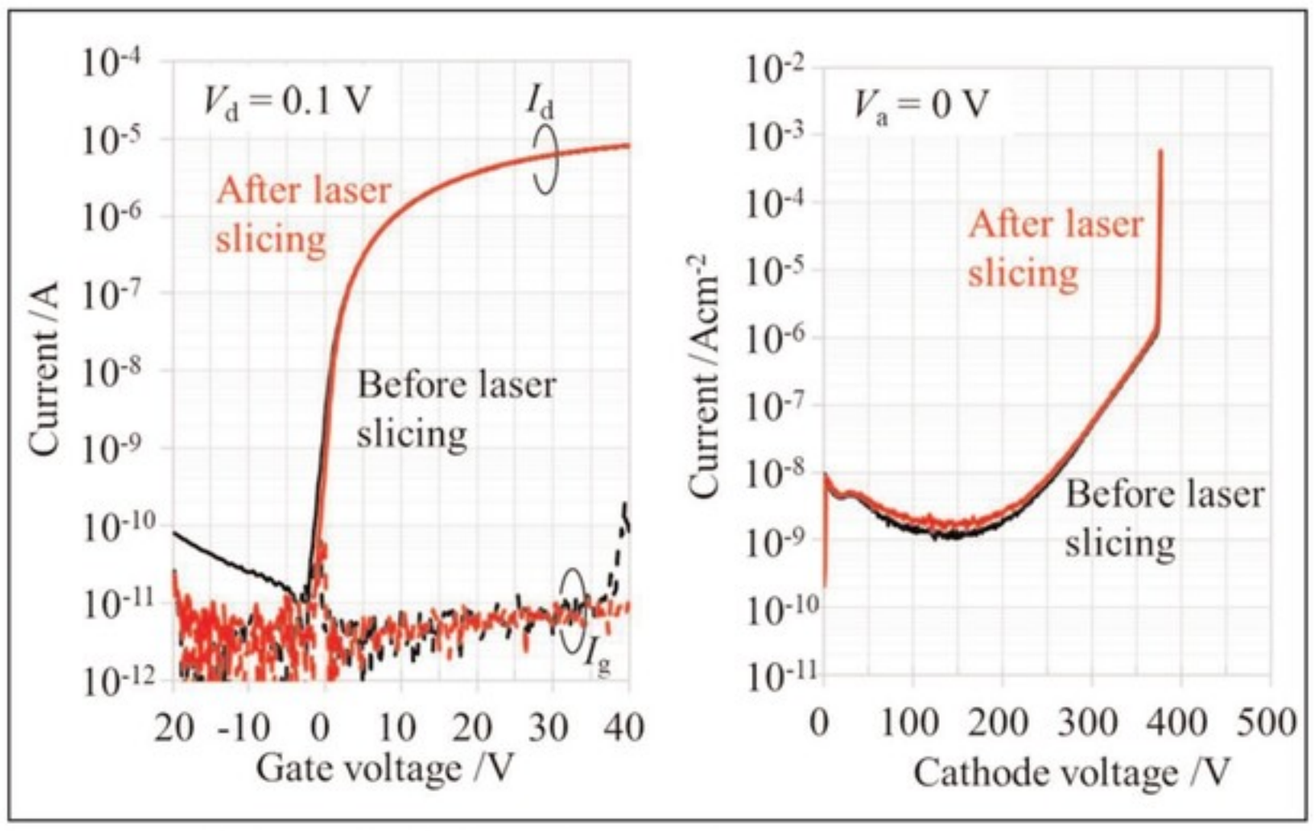

Figure 2. (a) Drain (I_d) and gate (I_g) current versus gate potential (V_g) for lateral MOSFET and (b) reverse curves of vertical PN diode before and after laser slicing.

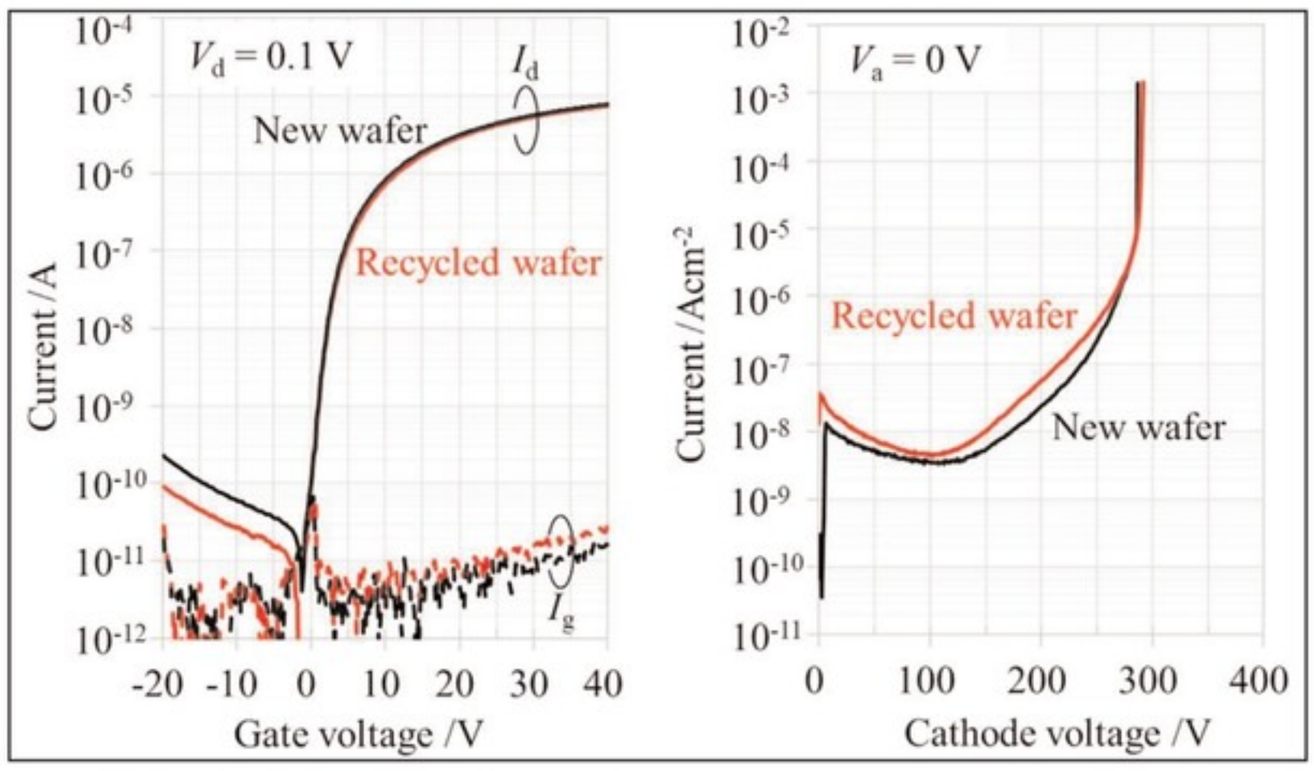

Figure 3. (a) Drain and gate leakage versus MOSFET gate potential for devices fabricated on new and recycled wafers. (b) Reverse leakage versus cathode voltage (V_c) of vertical PN diode.

The recycling process was verified by processing a recycled wafer along with a fresh wafer from the same supplier, simultaneously, both in terms of MOVPE and device fabrication (Figure 3). The recycled lateral MOSFET seems to have lower drain leakage in the OFF state (negative gate potential) but higher gate leakage at 40V. The recycled PN diode has a somewhat larger leakage under reverse bias.

The threshold voltages of the lateral MOSFETs were between −0.1V and +0.8V. The MOSFET channel mobilities were in the range 70–80cm^2/V-s. This is lower than reported vertical transistor mobilities in the range 173–266cm^2/V-s. ■

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