Reducing energy costs for AI and data processing

Chinese–German research has reduced SM-VCSEL energy per bit to 168fJ at 60Gbits/s.

Researchers based in China and Germany claim record energy efficiencies for high-speed, directly modulated 940nm single-mode vertical-cavity surface-emitting lasers (SM-VCSELs) [Mansoor A. Maricar, Appl. Phys. Lett., v126, p091101, 2025]. In particular, the energy per bit energy-to-data ratio (EDR) values are claimed to be the lowest reported to date for data rates up to 60Gbits/s. At the highest 60Gbits/s rate, the EDR was measured at 168 fJ/bit, while ~100fJ/bit could be achieved at 50Gbits/s.

The team members were associated with three Chinese institutions: the Bimberg Chinese–German Center for Green Photonics, the Key Laboratory of Luminescence Science and Technology, and the University of Chinese Academy of Sciences. One German institution was also involved: Technische Universität Berlin, where Dieter Bimberg has long been based.

The team was motivated by the explosion in energy usage driven by factors such as the four-orders-of-magnitude (104) increase in Internet users over the three decades covered by the 1990–2020 period. In turn, Internet power consumption does not just depend on number of users but is folded back on itself through social media, crypto-currency… and, most recently, the buzz around artificial intelligence.

The researchers comment: "Many of the technologies used on a daily basis, from language translation tools to virtual assistants to the growing accuracy of predictive text, are powered by advancement in artificial intelligence (AI), particularly in the area of natural language processing (NLP). The time and computer resources required to process vast amounts of text data make real-time analysis difficult. Specifically, data centers are experiencing a huge increase in energy demand due to the training of NLP models, which is far surpassing the rise of renewable energy sources."

The team used three epitaxial structures grown by metal-organic chemical vapor deposition on on-axis (001)-oriented gallium arsenide (GaAs) substrates. The optical confinement consisted of aluminium gallium arsenide ($Al_{0.12}Ga_{0.88}As/Al_{0.90}Ga_{0.10}As$) distributed Bragg reflectors (DBR) with compositionally graded interfaces. The n-doping and p-type doping were provided by silicon and carbon, respectively. The lower n-DBR mirror had 34 periods. The upper p-type mirrors were 18.5 periods for two of the designs (labeled B and C), or 22.5 periods (design A).

The active regions consisted of compressively strained $In_{0.17}Ga_{0.83}As$ quantum wells (QWs) embedded in $GaAs_{0.84}P_{0.16}$ barriers. Designs A and B had five QWs, while C had three. The designs aimed a high differential optical gain at low current density in a half-wavelength cavity.

The VCSELs also had a 3μm double oxide aperture provided by selective wet oxidation. The devices were planarized with 8μm photosensitive benzocyclobutene (BCB), reducing parasitics and enabling high-frequency contact pads. The top mesa was 21μm diameter.

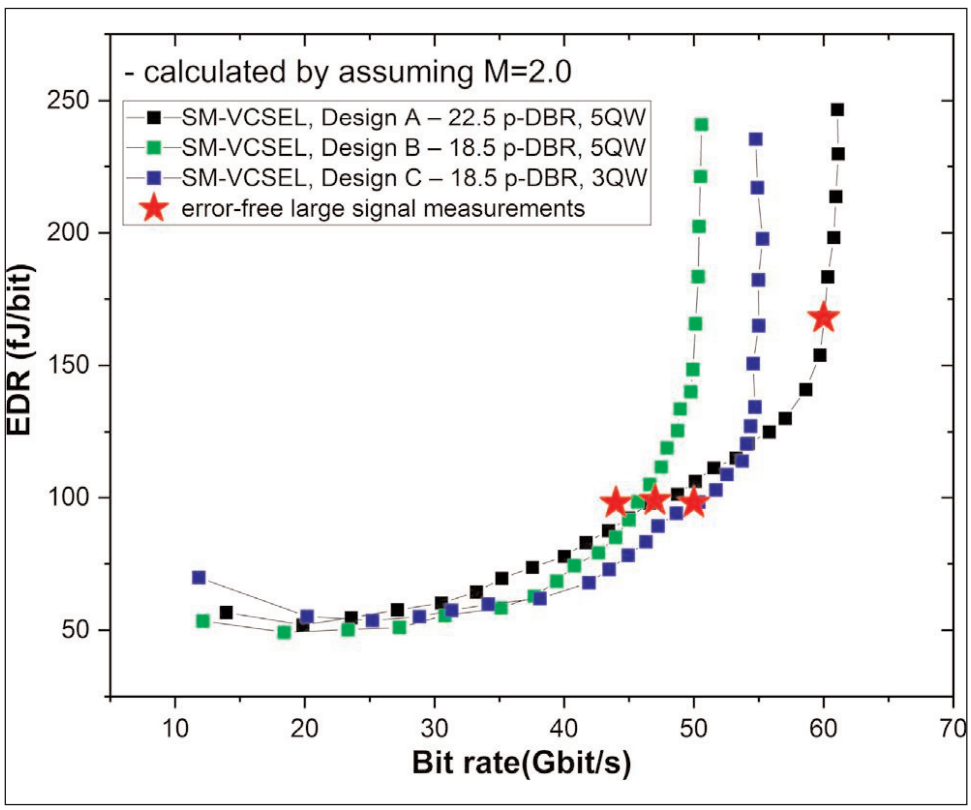

Figure 1. EDR as function of bit rate for different SM-VCSEL designs.

The researchers also shifted the cavity mode to be 15nm away from the quantum well active region gain peak, an "important design modification in comparison to some of our previous VCSEL designs".

The team explains: "The cavity modes permitted by a VCSEL cavity design are narrowly spaced. The strongest lasing mode is the one most closely matching the peak gain with the cavity mode. Thus, heating causes changes in the effective cavity length and the spectral position of the gain, having a big impact on intensity. Temperature has a comparable effect on the threshold current density, since rising temperatures decrease the quantum wells' gain. Since the temperature of the active area is always higher than that of the surroundings, a temperature-robust VCSEL needs significant differential gain at high active area temperatures."

The 15nm gain-to-etalon wavelength offset was expected to provide a smoother differential gain dependence on temperature in the 25–85°C range. Effective index optical model calculations gave photon lifetimes (τ_p) of 4.9ps for design A, and 2.5ps for the thinner top-DBR samples B and C.

The 3dB maximum bandwidths (f_{3dB}) from small-signal testing for VCSELs A–C were 30GHz, 26GHz and 28GHz, respectively. Theoretical considerations suggest that reducing photon lifetime should increase bandwidth. The team comments: "Although increasing differential gain or decreasing τ_p can improve the modulation bandwidth, τ_p has a non-monotonous relationship with the bandwidth, with an optimal point beyond which reductions are counter-productive." Design A, despite having the longest photon lifetime, also had the widest f_{3dB}.

The devices achieved threshold currents as low as 170μA and light output up to 1.43mW (Table a).

The researchers calculated expected EDRs for the three designs, using results from small-signal testing (Figure 1). The minimum came around 30Gbits/s, but the devices with short photon lifetimes increased more rapidly beyond that. Device A was expected to be able to work error-free, i.e. with a bit error rate (BER) around 10^{-12}, at 60Gbits/s. The calculated error-free data rates fell for B and C to 52Gbits/s and 56Gbits/s, respectively.

VCSEL-A achieved 60Gbits/s data rate with 2.4mA bias current and 168fJ/bit EDR (Figure 2), based on large-signal non-return-to-zero (NRZ) pseudo-random binary sequence (PRBS 2^7–1) modulation. Reducing the data rate to 47Gbits/s with 1.5mA bias enabled a 99fJ/bit EDR. Devices B (1.5mA bias) and C (1.7mA) achieved close to 100fJ/bit EDR for 44Gbits/s and 50Gbits/s data rates, respectively.

The higher bit rate for VCSEL-C for near 100fJ/bit EDR (Table b) is attributed at least in part to its reduced number of QWs. The researchers comment: "SM-VCSEL-C has three and SM-VCSEL-B has five QWs, thus B heats up faster for a given current and current saturation (maximum bandwidth) is reached at lower currents." ■

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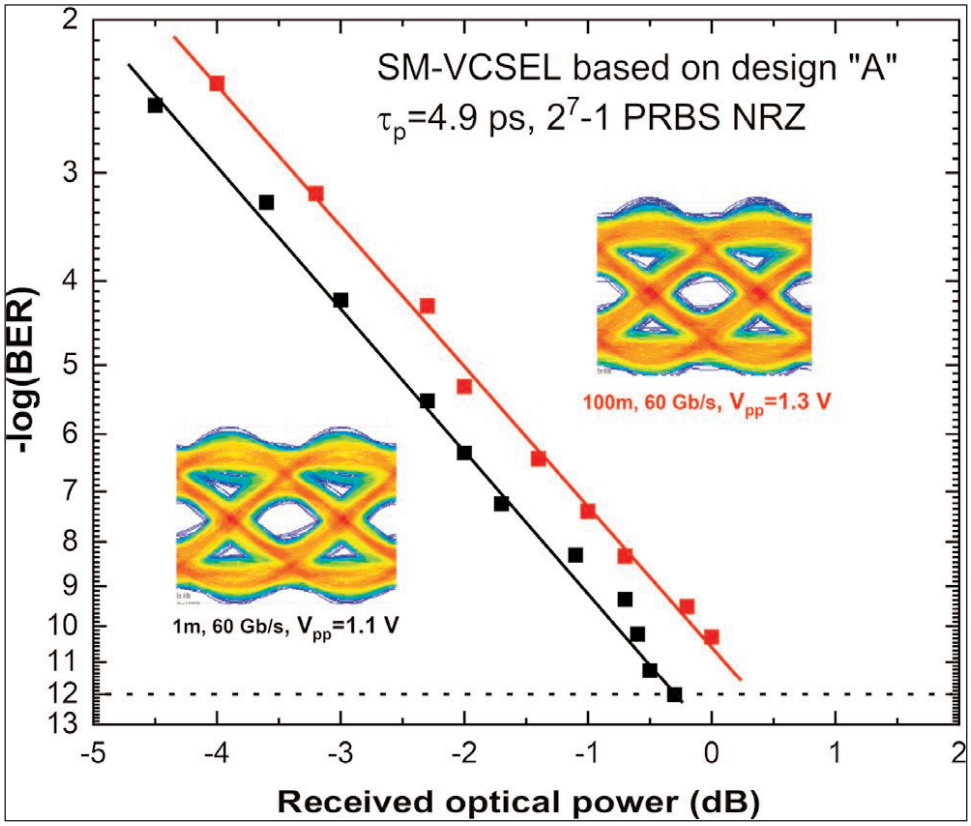

Figure 2. BER versus received optical power 60Gbits/s in 1 and 100m OM5 fiber for SM-VCSEL-A.

Table 1. Typical light–current–voltage properties.

Device	Threshold	Maximum output power
A	170μA	0.91mW @ 4.1mA
B	360μA	1.43mW @ 4.0mA
C	260μA	0.84mW @ 3.9mA

Table 2. Summary of SM-VCSEL data rate and EDR performance.

Device	Data rate	Bias current	EDR
A	60Gbits/s	2.4mA	168fJ/bit
A	47Gbits/s	1.5mA	99fJ/bit
B	44Gbits/s	1.5mA	98fJ/bit
C	50Gbits/s	1.7mA	98fJ/bit