Vertical power & high-speed III–V devices show their promise

Mike Cooke reports on presentations at International Electron Devices Meeting (IEDM 2017) in San Francisco (2–6 December).

Compound semiconductor materials for power and high-speed applications continue to have fair representation among the contributions at the year-end IEDM. Combining group-III metals — gallium (Ga), indium (In) and aluminium (Al) — with group-V elements — nitrogen (N), arsenic (As), phosphorus (P), antimony (Sb) — offers a huge palette of electronic and thermal behaviors that can be harnessed in modern and future technology.

At the most recent IEDM, one theme from the power and high-speed sections was the use of vertical devices, which can offer advantages in terms of smaller footprints and hence more compact electronics. At the same time, lateral devices continue to be developed and improved. Finally, researchers are seeking to combine light emitting devices with low-cost silicon photonics.

Here, we report on some of these developments. Next issue, we plan to look beyond the near future to IEDM presentations on the prospects for the two-dimensional (2D) electronics of thin layers provided by materials such as graphene, dichalcogenides, black phosphorus, etc.

Vertical power

At IEDM, Fuji Electric Co Ltd and Japan's National Institute of Advanced Industrial Science and Technology (AIST) proposed a vertical gallium nitride (GaN) Schottky barrier diode (SBD)-wall-integrated trench metal-oxide-semiconductor field effect transistor (SWITCH-MOS, Figure 1) structure to solve issues from PiN body diodes such as forward degradation and reverse recovery loss [session 9.1].

The design enabled a small 5μm cell pitch and 1.2kV operation while successfully inactivating the PiN-diode without degradation of on- and off-state characteristics. The freewheeling PiN diode is aimed at protecting the transistor from voltage spikes. The small cell size is helpful from the perspective of not adding unduly to on-resistance by the inclusion of an extra SBD. The on-resistance and blocking performances were similar to those of conventional power MOSFETs with U-shape trench (UMOS) without an integrated Schottky barrier diode, according to the team.

Massachusetts Institute of Technology in the USA, the Singapore–MIT Alliance for Research and Technology, and RF LLC and Columbia University in the USA have claimed record performance from a normally-off GaN vertical transistor (Figure 2) with +1V threshold [session 9.2]. The device features submicron fin-shaped channels and uses only n-GaN layers without resistive p-GaN or costly, complex epitaxial regrowth processes.

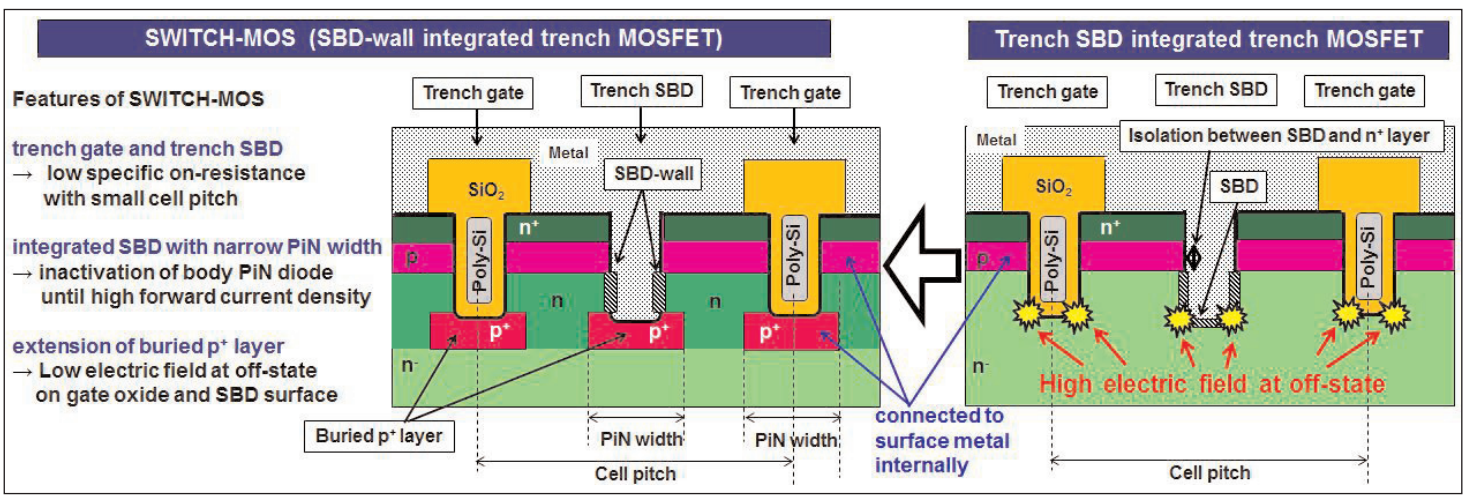

Figure 1. Schematic cross-sectional illustration and features of SWITCH-MOS.

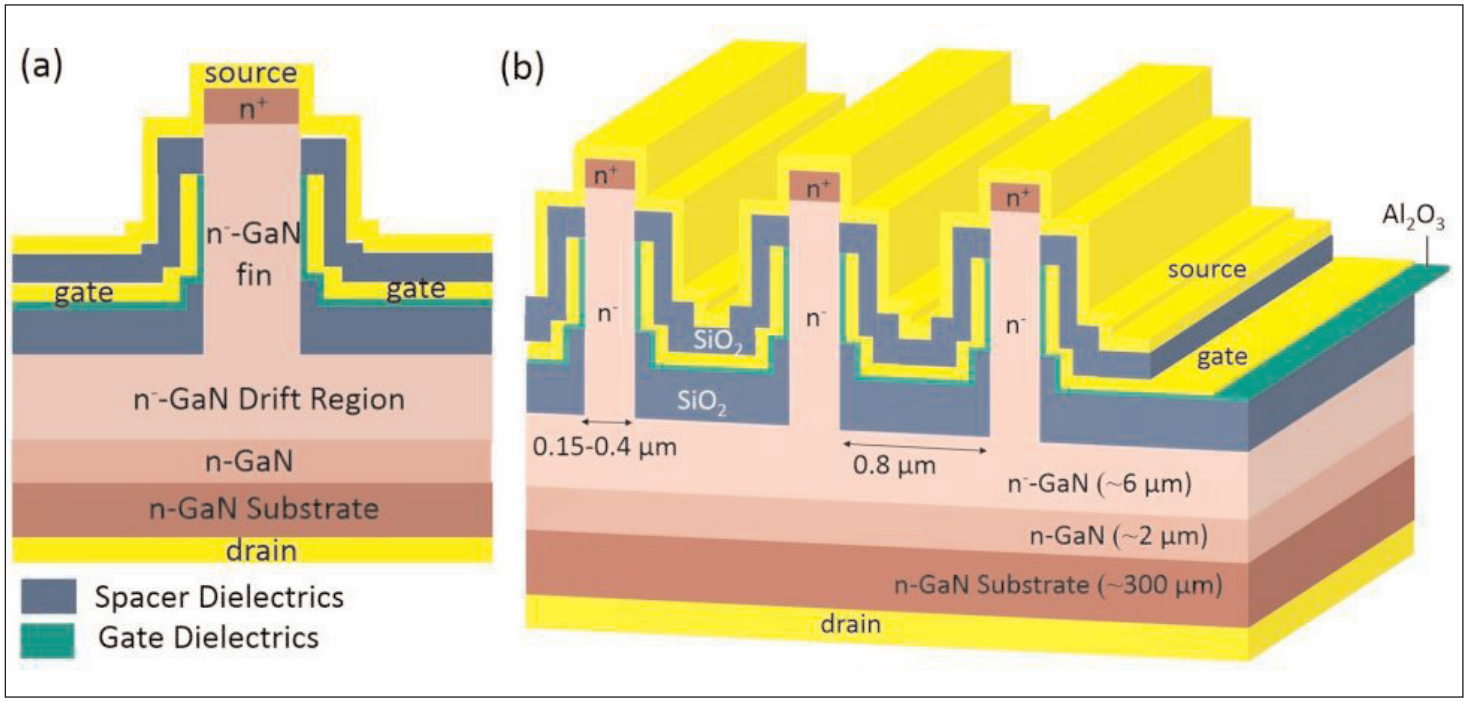

Figure 2. (a) Cross-sectional schematic of device fin unit-cell and (b) side-view three-dimensional schematic of proposed vertical GaN fin power FETs with multiple fins. Fin length ~1µm in vertical direction.

The specific on-resistance (R_{on}) was 0.2mΩ-cm^2 fin area and 1mΩ-cm^2 device area. The on/off current ratio was around ten orders of magnitude. The breakdown voltage (BV) for 10^{-4}A/cm^2 current leakage was more than 1200V. In the on-state, currents reached 10A for a large 0.8mmx0.55mm device or 25kA/cm^2 density in smaller devices. The Baliga figure of merit (BV^2/R_{on}) reached 7.2GW/cm^2 for fin area normalization and 1.44GW/cm^2 for device area. These figures are claimed to be the "best in all reported normally-off GaN transistors".

The researchers comment: "The R_{on} of our vertical fin power FETs normalized to total device area can be further reduced by reducing the lateral distance between fins and increasing the fin aspect ratio, while the BV can be further improved by incorporating multiple gate and source field plates to smoothen the peak E-field at the gate edge."

The transistors work by depleting the n-GaN material due to its work function difference with the molybdenum gate metal on the two free surfaces of the fins, blocking current flow at 0V gate potential. As the gate potential increases, electrons accumulate at the n-GaN/aluminium oxide dielectric interfaces, opening up two channels for current flow. The epitaxial structure was grown by metal-organic chemical vapor deposition (MOCVD) on freestanding GaN.

University of California Davis (UCD) and University of California Santa Barbara (UCSB) in the USA have used a double-field plate design to create a vertical GaN open-gate FET (OG-FET) with up to 1435kV blocking 50mA/cm^2 current density, low specific on-state resistance of 2.2mΩ-cm^2, and normally-off +4.7V threshold [session 9.4].

The device (Figure 3) used a 10nm MOCVD regrown GaN channel layer to reduce resistance. The rest of the structure was grown by commercial epitaxy foundry IQE by MOCVD on freestanding GaN. The regrown layer had 2x reduced contact and sheet resistance, compared with an in-situ-grown layer. The improvement was attributed to an acid treatment before the regrowth, aimed at inhibiting the diffusion of the magnesium doping of the p-GaN layer.

A large-area 0.4mmx0.5mm transistor using the technology featured a 900V breakdown voltage and 4.1Ω on-state resistance. The average channel electron mobility was 185cm^2/V-s.

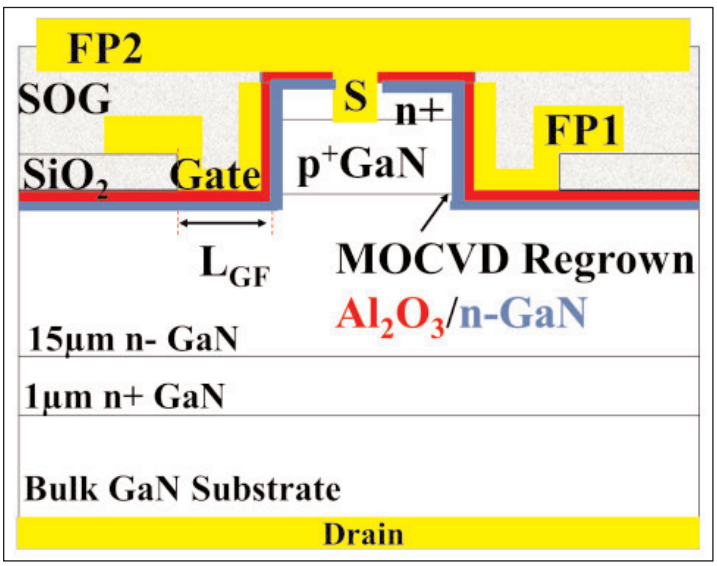

Figure 3. Schematic cross section of GaN OG-FET with double field-plate structure.

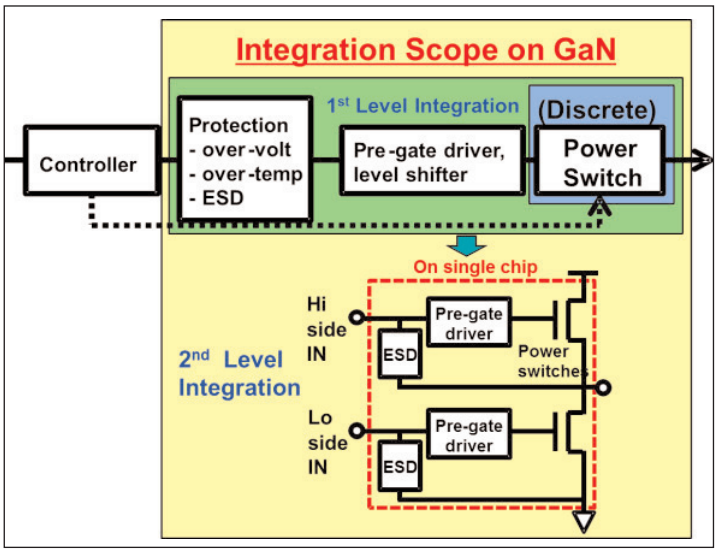

Figure 4. Expanding scope of GaN-on-Si integration.

Lateral GaN

Taiwan Semiconductor Manufacturing Company presented its view on the 'next stage' for GaN power devices integrated with peripheral low voltage active and passive devices on silicon (Si) [session 33.1]. According to TSMC this involves two levels: first, protection/control/driving circuits; second, adding high/low-side on-chip integration to a 100V technology platform (Figure 4). The scheme would eliminate channel modulation due to substrate bias sharing, along with wiring parasitics.

The team fabricated enhancement-mode FETs (E-) and depletion-mode (D-) metal-insulator-semiconductor FETs on 6-inch GaN-on-Si wafers. The E-FET ratings were 100V and 650V, while the D-FETs were rated at 650V. The researchers also developed 12V E/D-HEMTs rectifiers, 2DEG resistors, and capacitors as part of the 1st-level development.

An electrostatic discharge circuit achieved more than 5kV surge sustainability. A DC–DC buck step-down converter operating at 800kHz showed on-resistance reduced by ~25% by biasing the bulk semiconductor dynamically rather than setting it at the ground potential.

University of Padova, ON Semiconductor, and CMST imec/Ghent University have used 3MeV proton irradiation to reduce dynamic on-resistance to zero in GaN power HEMTs [session 33.5]. The researchers claim their work as the first demonstration of the effect.

Negative charge ionizing the carbon (C) acceptors reduces the drain current, which increases dynamic resistance after exposure to high off-state bias. By contrast, positive charge in the buffer increases drain currents. The proton irradiation enables more efficient electron detrapping by providing leakage from the buffer to the 2DEG channel in the off-state (Figure 5). The researchers write: "Since the C-doped GaN is highly resistive, the increase in the conductivity of the uid[unintentionally doped]-GaN layer does not lead to an increase in the drain and vertical leakage current."

The static characteristics of the devices such as threshold voltage were not affected up to $1.5x10^{14}/cm^2$ proton fluence. However, high irradiation at the $10^{15}/cm^2$ level shifted the threshold +2V. At $1.5x10^{14}/cm^2$ fluence, the dynamic on-resistance was completely suppressed in 600V/150ºC operation, according to the team.

Massachusetts Institute of Technology has been working to improve linearity of GaN-based high-electron-mobility transistors (HEMTs) using fin-like structures to give transconductance compensation [session 25.3]. The fins allow different threshold voltages across the device that can increase linearity, as desired for 5G-LTE, WIMAX, Sat-Com, CAT-TV and radar applications. The researchers used Wolfspeed's GaN-on-SiC fabrication process on wafers from IQE to create two parallel 250nm GaN HEMTs. Some of the resulting devices achieved 20dB reduction in harmonics and 6dB increase in the third-order output intercept point (OIP3), compared with a baseline device without compensation.

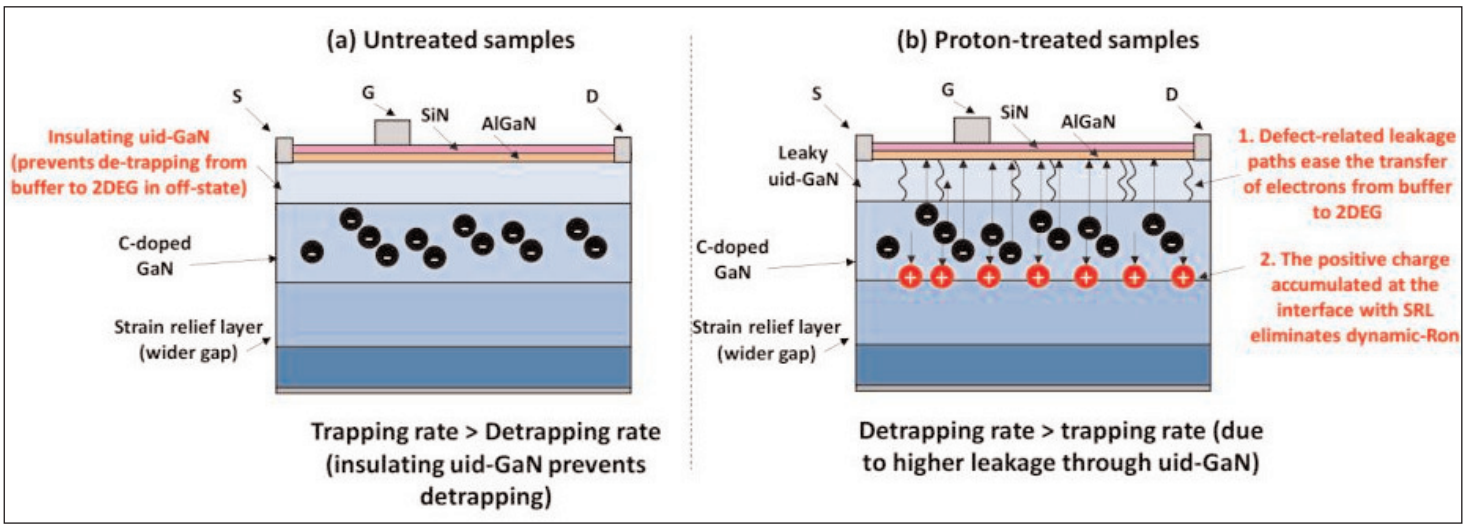

Figure 5. Schematic of effect of proton irradiation.

High-speed nanowires

KU Leuven, IMEC and Lam Research Belgium claimed record performance from indium gallium arsenide ($In_{0.53}Ga_{0.47}As$) vertical nanowire (VNW) and nanosheet gate-all-around FET and transmission line measurement (TLM) devices [session 17.1]

The top-down VLSI-compatible fabrication (Figure 6) scaled the effective oxide thickness and used ammonium sulfide ($(NH_4)_2S$) passivation and hydrogen/nitrogen 'forming' gas annealing to improve device performance. The researchers also claim the first TLM structures on top-down n-type $In_{0.53}Ga_{0.47}As$ vertical nanowire arrays. Such structures are used to study contact resistance contributions.

A range of gate oxide layers were tested, but the best performing involved passivation before atomic layer deposition of 1nm aluminium oxide and 3nm hafnium dioxide. The capacitive equivalent thickness of the dielectric was 1.62nm.

One device with 45nm NWs achieved an off current as low as 100pA/μm with 0.5V drain bias. and a Q value (transconductance/subthreshold swing) of 16. Reducing the diameter to 30nm gave a subthreshold swing of 63mV/decade, which is described as the best reported in the literature for any type of III–V device.

Forming gas annealing increased the Q to 21 with a peak transconductance (G_{mMAX}) of 1.6mS/μm. "These values for G_{mMAX} and Q are the best reported in literature for vertical III–V device and are only outperformed by lateral devices due to the contact resistance penalty at the VNW top," the team comments.

The forming gas anneal did, unfortunately increase the off-current to 100nA/μm. On the plus side, the on-current was 397μA/μm, also claimed as a record. The forming gas anneal is thought to reduce the Schottky barrier and contact resistance between the InGaAs and molybdenum used as the top contact.

Vertical device configurations can offer more compact footprints, compared with the mainstream planar structures. The vertical format could also allow longer gate lengths, which could be beneficial for high-mobility III–V compound semiconductor devices with hard-to-control off-current leakage.

Massachusetts Institute of Technology [session 17.2] also claimed records, this time for the "first" sub-10nm-diameter VNW MOSFETs "of any kind in any semiconductor system". Reactive ion etch, alcohol-based digital etch and Ni alloyed contacts were used to fabricate top-down InGaAs MOSFETs (Figure 7).

Records for a 7nm-diameter device included an on-current of 350μA/μm with off-current 100nA/μm in 0.5V operation. Other characteristics of the device were a peak transconductance of 1.7mS/μm, also claimed as a record, and minimum subthreshold swing (SS) of 90mV/dec, giving a maximum Q factor of 19, the highest reported in vertical nanowire transistors, according to the team (but apparently beaten by the presentation just above).

The researchers see the 7nm diameter (D) as being the 'design point' for a future 5nm technology node. "A remarkable result, is that the performance of these devices continues to improve as D shrinks, with a record g_m achieved at D=7nm," they add.

The team had previously used water-based digital etch but had found that surface tension effects had resulted in nanowire breakage when attempting to reduce diameters below 10nm. By contrast, sulfuric acid (H_2SO_4) in methanol enabled fabrication of 5.5nm-diameter wires with 90% yield.

The nickel alloying involved the formation of highly

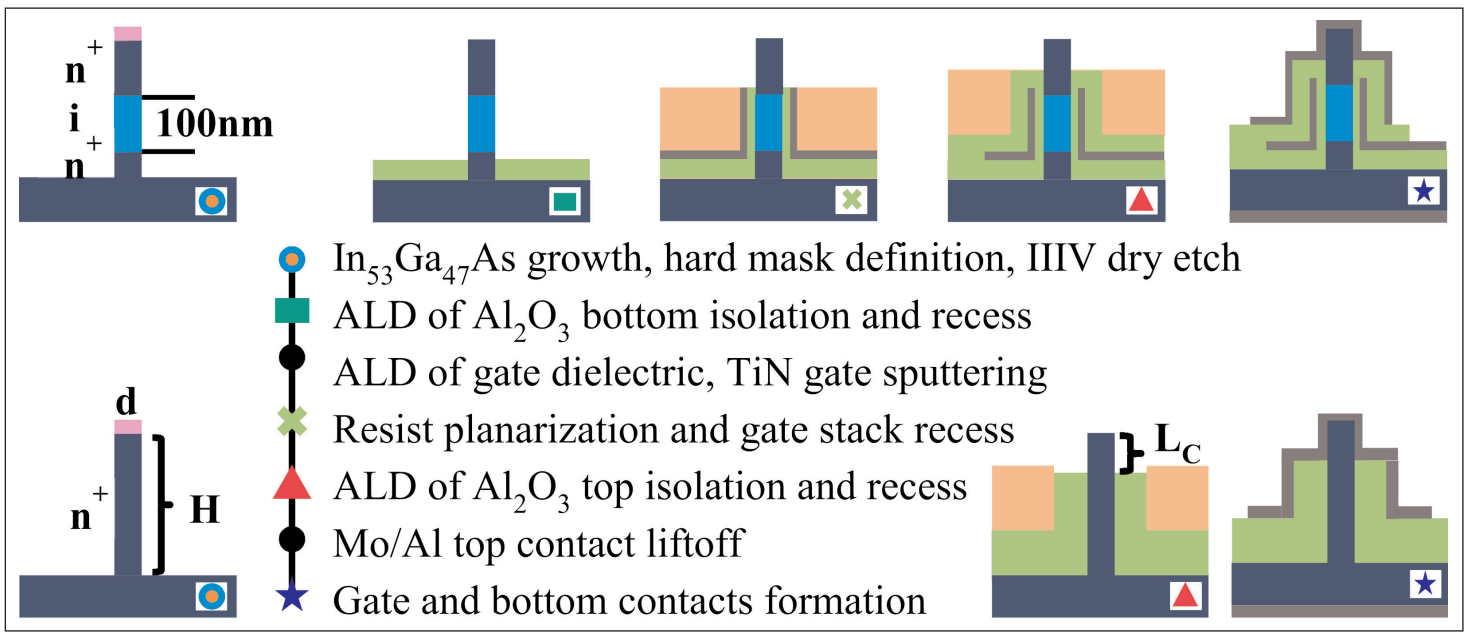

Figure 6. Key process steps from both VNW FET (top row) and VNW TLM (bottom row); d, H and L_C are NW diameter, NW height and contact opening length, respectively.

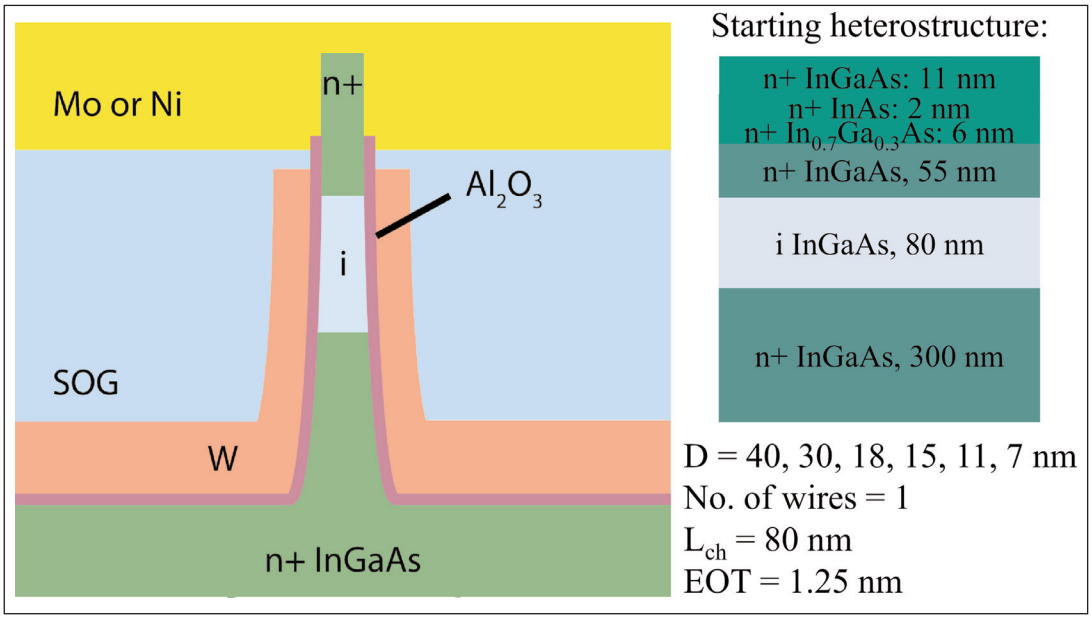

Figure 7. Schematics of device cross section, starting heterostructure and design parameters.

conducting NiInGaAs, avoiding molybdenum/tungsten mushroom-shaped top contacts, which can increase fragility and makes processing more complicated. The reported devices had an 80nm channel length. A forming gas anneal was also found useful in boosting on-current and gate control.

Lund University have boosted the transconductance of InGaAs VNW MOSFETs on Si to 2.4mS/μm [session 17.3]. The devices had gate lengths ranging from 25nm to 140nm. One device achieved an on-current of 407μA/μm at 100nA/μm off-current with 0.5V operation, also claimed as a record.

The nanowires were grown by MOCVD using gold seed particles on an InAs layer. The wires consisted of 100nm InAs, 100nm $In_{0.5}Ga_{0.5}As$, 300nm highly doped $In_{0.5}Ga_{0.5}As$. The doped $In_{0.5}Ga_{0.5}As$ also forms a shell around the unintentionally doped $In_{0.5}Ga_{0.5}As$. The core was approximately 30nm wide and the total core/shell structure was 50nm.

Fabrication involved electron-beam lithography on spin-coated hydrogen silsesquioxane (HSQ) resist. Different electron doses allowed different gate lengths to be achieved by varying the amount of top metal residue and thickness of spacer (Figure 8). The gate region was defined with digital etch that removed the shell region. The gate stack consisted of aluminium oxide/hafnium dioxide and tungsten metal.

The Q value also seems good at 22 on the basis of a peak transconductance of 1.9mS/μm and SS at 86mV/decade.

High speed FinFETs

IBM Research GmbH Zürich Laboratory, Switzerland, University of Udine, Italy, and ETH Zurich, Switzerland, achieved a claimed record of 249μA/μm for a 13nm-long replacement-metal-gate InGaAs-on-insulator n-FinFET on Si [session 17.5]. The fixed off-current was 100nA/μm at 0.5V drain bias.

The fin width was 17nm, while the 13nm gate length is seen as a target for sub-7nm technology nodes.

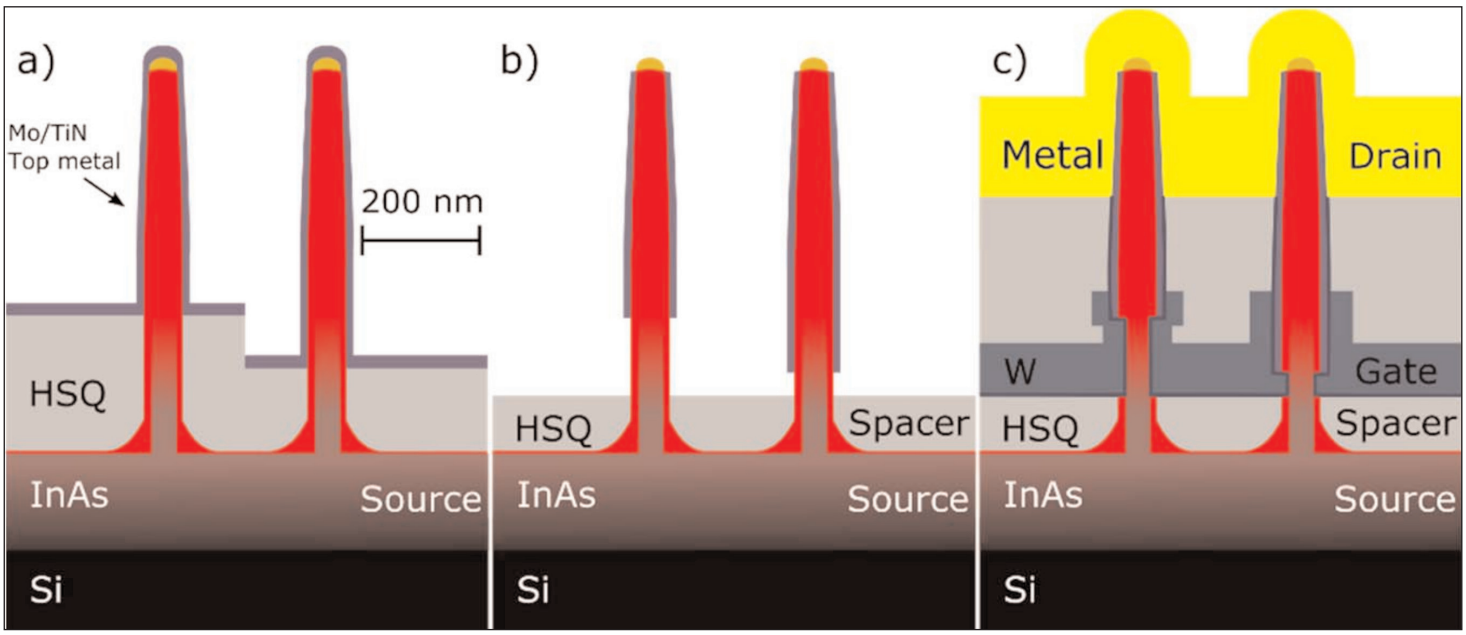

Figure 8. Fabrication after top metal deposition (a), first spacer deposition (b) and final contacts (c).

The 20nm InGaAs channel material was wafer bonded to the silicon. Regrowth was used to give raised source–drain material for lower access resistance (Figure 9). The gate stack used aluminium oxide and hafnium dioxide with 1.25nm capacitive equivalent thickness. Titanium nitride provided the work-function-defining metal, followed by tungsten fill.

Massachusetts Institute of Technology and Korea Institute of Science and Technology presented the first use of digital etch (DE) on indium gallium antimonide (InGaSb) transistors of any kind, enabling the first finFETs with widths down to 10nm [session 17.7]. The self-aligned devices (Figure 10), with ohmic contacts fabricated first, managed a transconductance of 160μS/μm at 0.5V drain, claimed as a record. The channel height was 23nm, giving a height/width aspect ratio of 2.3. Normalized according to fin width, the specific transconductance was 704μS/μm.

Antimonides have high hole mobility, creating opportunities for these materials as the p-type component of complementary MOS (CMOS) circuitry, while arsenides have high electron mobility. However, antimonides have processing challenges arising from their high chemical reactivity. Apart from the digital etch, the researchers also used nickel ohmic contacts.

The digital etch involved exposure to oxygen at room temperature for three minutes and 30s wet etching in hydrochloric acid in isopropyl alcohol. The digital etch was performed after reactive ion etch, giving fins down to 15nm wide.

The heterostructure was grown by molecular beam epitaxy on semi-insulating GaAs. The hole mobility was measured at 1175cm^2/V-s.

The researchers admit that the turn-off characteristics of the finFETs are presently "insufficient", but "nevertheless, the results here represent a significant improvement over earlier InGaSb FinFETs due to the new DE technique."

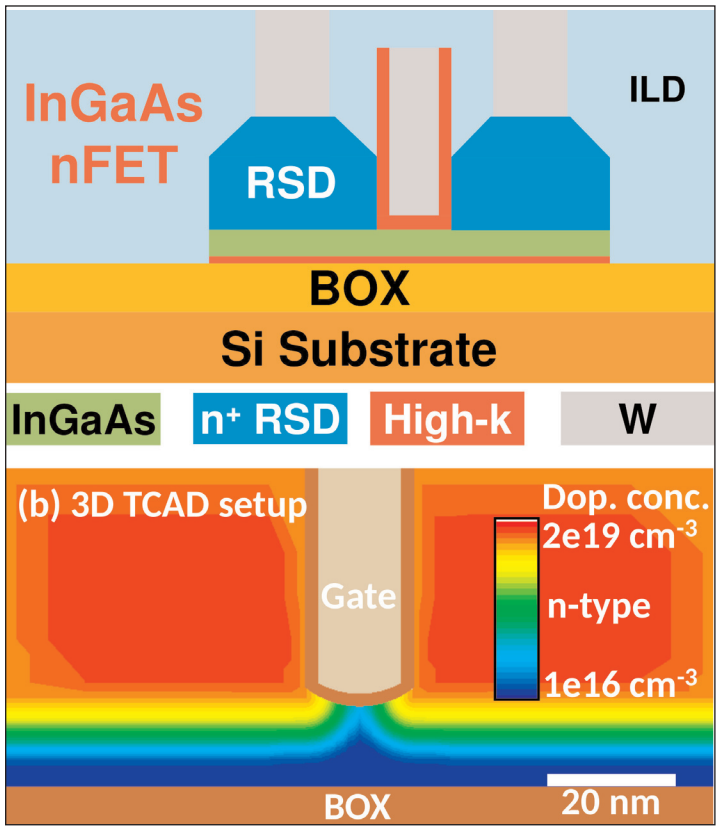

Figure 9. (a) Cross-sectional schematic of self-aligned spacer-free replacement metal gate InGaAs-on-insulator devices; (b) three-dimensional simulation setup shown across gate with doping profile.

Optoelectronics on silicon

University Grenoble Alpes and STMicroelectronics presented the "first integrated hybrid III–V/Si laser in a fully CMOS-compatible 200mm technology" [session 24.1]. The III–V epitaxial material was directly bonded with 100nm silicon dioxide interlayer to the silicon-on-insulator (SOI) substrate (Figure 11). The SOI wafer was prepared by adding to the 310nm to silicon layer to make a 500nm-thick waveguide structure in the region of the

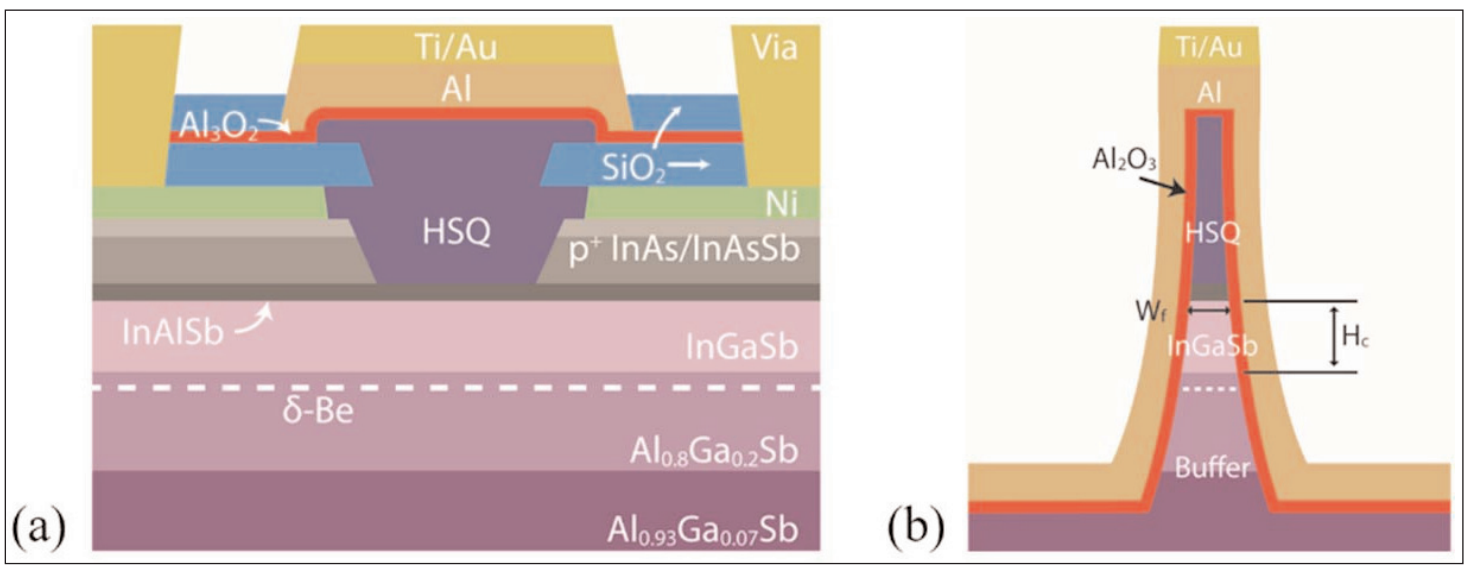

Figure 10. Schematic FinFET cross sections (a) along and (b) across fin.

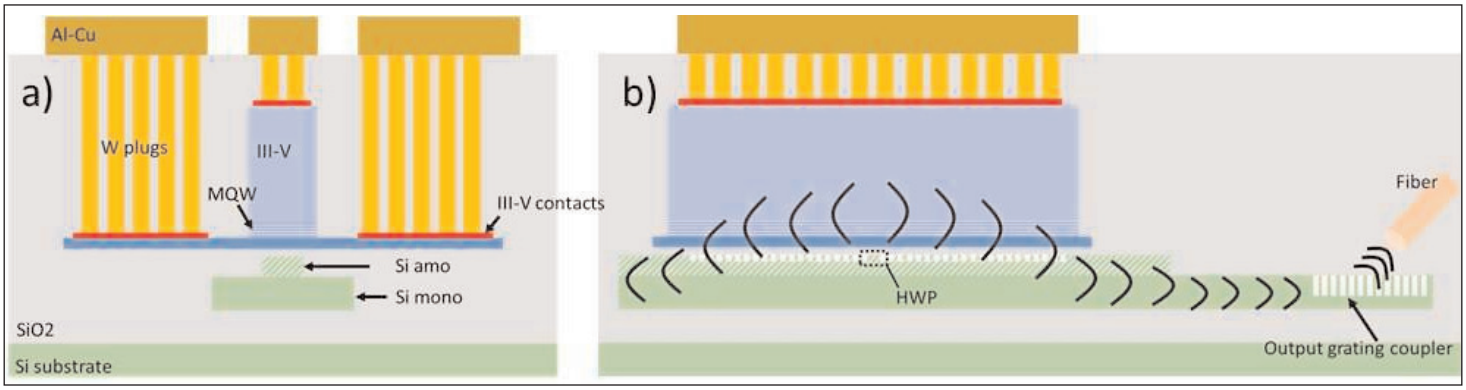

Figure 11. Transversal (a) and longitudinal (a) schematic views of laser. Active region consists of InGaAsP multiple QWs surrounded by p- and n-doped InP layers.

laser. A half wave plate (HWP) distributed feedback (DFB grating) was etched along the silicon waveguide. Since gold is unwanted in CMOS processing facilities, the researchers used nickel contacts instead.

The side mode suppression ratio (SMSR) of the laser reached 50dB and the maximum output power coupled into the waveguide was 4mW. The 1300nm central wavelength of the laser emission was slightly offset from the optimum of the output grating coupler, which resulted in power loss. The fabrication flow is fully planar and compatible with large-scale integration of silicon photonics circuits.

University of Stuttgart and University of Massachusetts reported "the first demonstration" of a germanium directly tunnel-modulated LED/laser light source on (100)Si [session 24.4]. The source was part of a silicon photonic device that emitted light under reverse bias and detected under zero/forward bias. The emission and detection used low-voltage switching tunnel Zener/Esaki tunnel diodes (TDs).

The team claims: "The devices enable for the first time monolithic, highly efficient electrical-to-optical (E/O; C_S = 114mV/dec) and optical-to-electrical (O/E; C_S = 31mV/dec) signal conversion since the TDs control carrier injection and extraction."

The LED achieved modulation frequencies of 1GHz. With a laser cavity, output power reached 1.6mW with added optical pumping from a supercontinuum lamp injector. The wavelength was in the range 1670–1690nm.

Band-to-band tunneling was used to inject electrons into the higher energy direct valley of the conduction band structure, enabling light emission in the indirect Ge semiconductor material (Figure 12). ■

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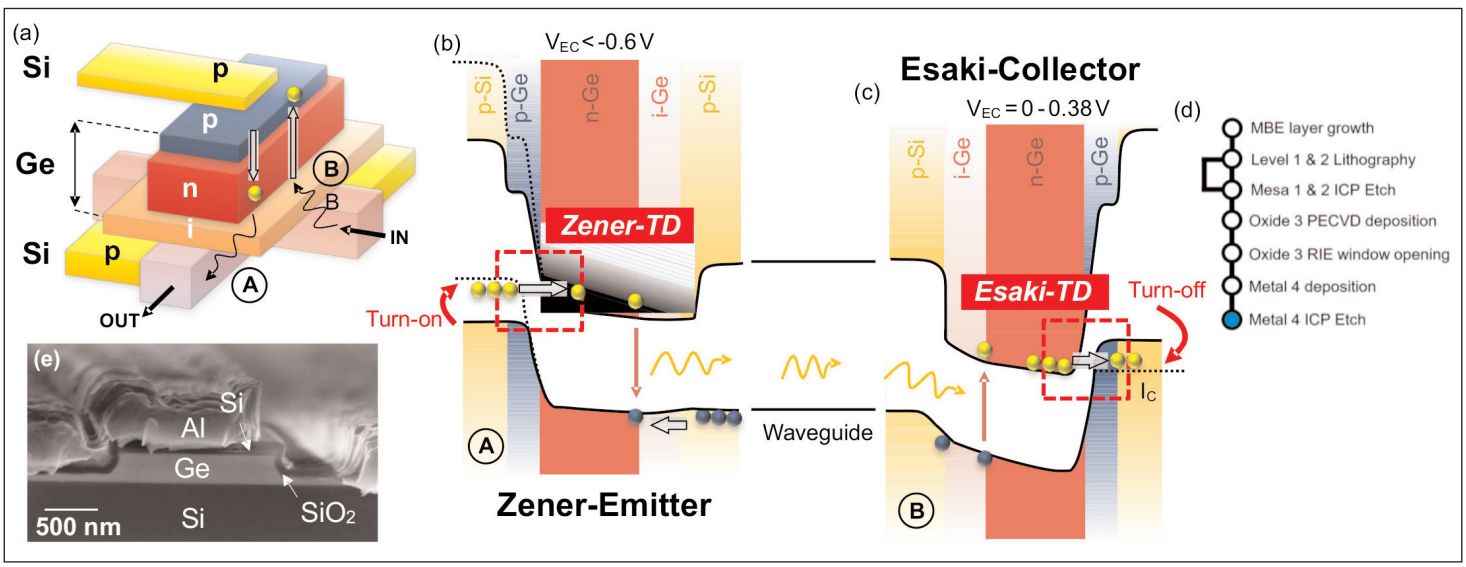

Figure 12. (a) Schematic of Zener-emitter/Esaki-collector monolithic photonic device. (b) Electrons injected by reverse biased Ge p–n Zener tunnel diode to direct conduction, while holes drift from forward biased n–i–p diode, creating modulated, in-plane optical response, which can be transferred by Si waveguide. (c) Light absorbed in i-Ge of zero biased Esaki-collector. Generated electrons drift to n–p Esaki diode collector. (d) CMOS process compatible process sequence and (e) scanning electron microscope image of device.