

# TSMC's GaN-on-Si patents supporting ST's strategic move towards power GaN adoption in automotive use

At least 12 key TSMC inventions relate to GaN-on-Si power applications.

**A**s announced in February, STMicroelectronics of Geneva, Switzerland is collaborating with Taiwan Semiconductor Manufacturing Corporation (TSMC, the world's biggest silicon wafer foundry) to accelerate the development of gallium nitride (GaN) technology for power applications, and more specifically for automotive applications (converters and chargers for hybrid and electric vehicles).

With this recent manufacturing partnership, STMicroelectronics has joined the series of companies that have trusted TSMC for volume production of GaN power devices, including market leader GaN Systems, as well as VisIC and Navitas Semiconductor (focusing on GaN power IC technology). STMicroelectronics will begin by sampling discrete GaN power devices, to be followed soon by GaN IC products based on TSMC's GaN-on-Si process technology.

TSMC's GaN-on-Si technology was reviewed in Knowmade's 'GaN-on-Si Patent Landscape Analysis' (released in January), which covers about 40 patent families (inventions) related to this technology, regrouping more than 130 patents filed worldwide, mainly in US (70+) and China (25+).

"TSMC has leading GaN-on-silicon manufacturing expertise, and we have identified at least 12 key

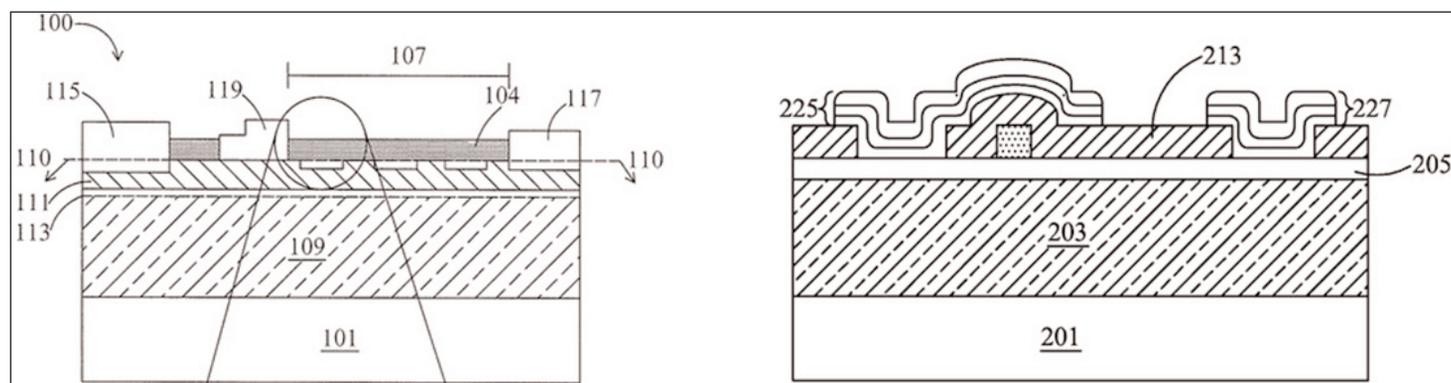
inventions narrowly related to power applications," says Remi Comy PhD, Knowmade's technology and patent analyst, Compound Semiconductors and Electronics. Indeed, TSMC was actively filing GaN-on-Si patents for power applications between 2012 and 2017 and has strongly focused on the USA (20+ granted patents).

The patent portfolio protects technological approaches providing improved GaN-on-Si buffer resistivity, using three main approaches:

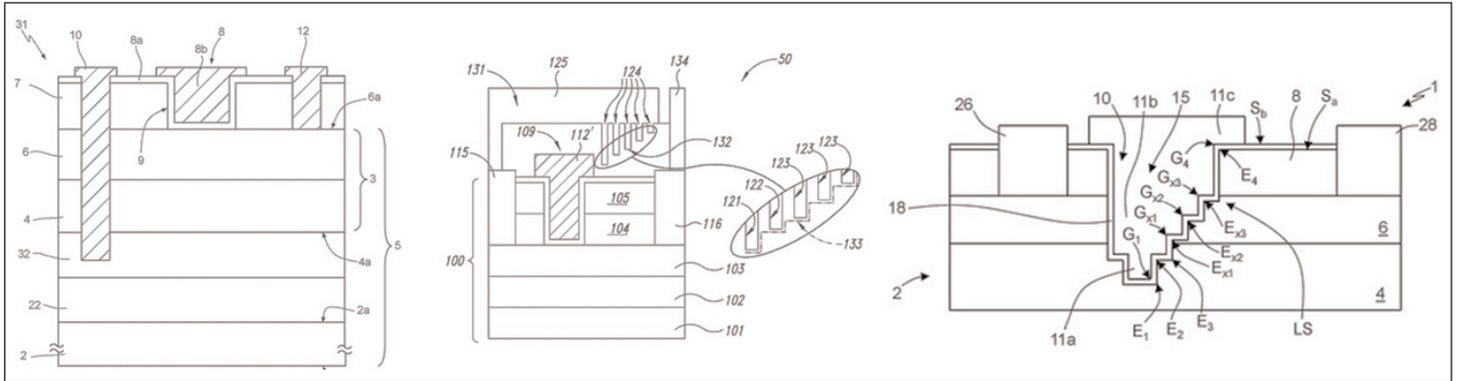
- p-type conductivity dopants in graded buffer layers and ungraded buffer layers (US patent 8,791,504);
- diffusion-blocking layer between the buffer layer and the silicon substrate (US patent 9,245,991);
- multi-strained superlattice structures (SLS) to overcome the limitations due to carbon doping of the buffer layers (US patent 10,109,736).

Next, TSMC focused its patenting activity on removing the breakdown voltage limitations due to the surface gate-drain region, inserting buried dielectric portions in the AlGaN barrier (Figure 1a), in addition to the use of field-plate structures (Figure 1b) and an AlGaN barrier with Al-graded composition (US patent 10,522,532).

Interestingly, TSMC's latest GaN-on-Si developments for power applications focused on the fabrication of GaN power integrated circuits (ICs) via US patent



**Figure 1: (a) GaN HEMT with one or more dielectric plug portions in the barrier between the gate and the drain (US patent 8,884,308). (b) Substrate breakdown voltage improvement for group III-nitride on silicon substrate (US patent 9,111,904).**



**Figure 2: Normally-off structures patented in 2017-2018 by STMicroelectronics (US patents 10,566,450, 10,050,136 and 10,522,646).**

9,793,389, related to the isolation of adjacent GaN-on-Si power devices, and US patent 10,522,532 related to the formation of through-GaN vias (TGVs).

In the ‘GaN-on-Si Patent Landscape Analysis’, Knowmade also analyzed the patent portfolio of STMicroelectronics, which is still strengthening its IP position in the power GaN patent landscape. In 2017–2018, ST focused on GaN device technology, especially normally-off transistor structures (Figure 2).

STMicroelectronics’ normally-off transistor structures (US patents 10,516,041, 10,566,450 and 10,522,646) are based on a tri-layer epitaxial stack NiO/AlGaN/GaN, the selective removal of NiO in the gate region and the deposition of a gate dielectric (AlN, Al<sub>2</sub>O<sub>3</sub> or SiO<sub>2</sub>) on the AlGaN barrier (with or without recess). The buffer region may include a first carbon-doped buffer layer for increasing the breakdown voltage and a second p-type buffer layer for limiting the degradation of dynamic on-resistance due to the first buffer layer. It can be combined with the presence of a sloped field plate in order to further reduce dynamic on-resistance phenomenon, implemented with the advantageous method described in US patent 10,050,136.

Previously — in 2018 — STMicroelectronics started a joint R&D program with The French Alternative Energies

and Atomic Energy Commission (CEA), focused on the development of GaN power devices on 200mm silicon substrates, in view of establishing a pilot manufacturing line in 2020 in STMicroelectronics’ foundry in Tours, France.

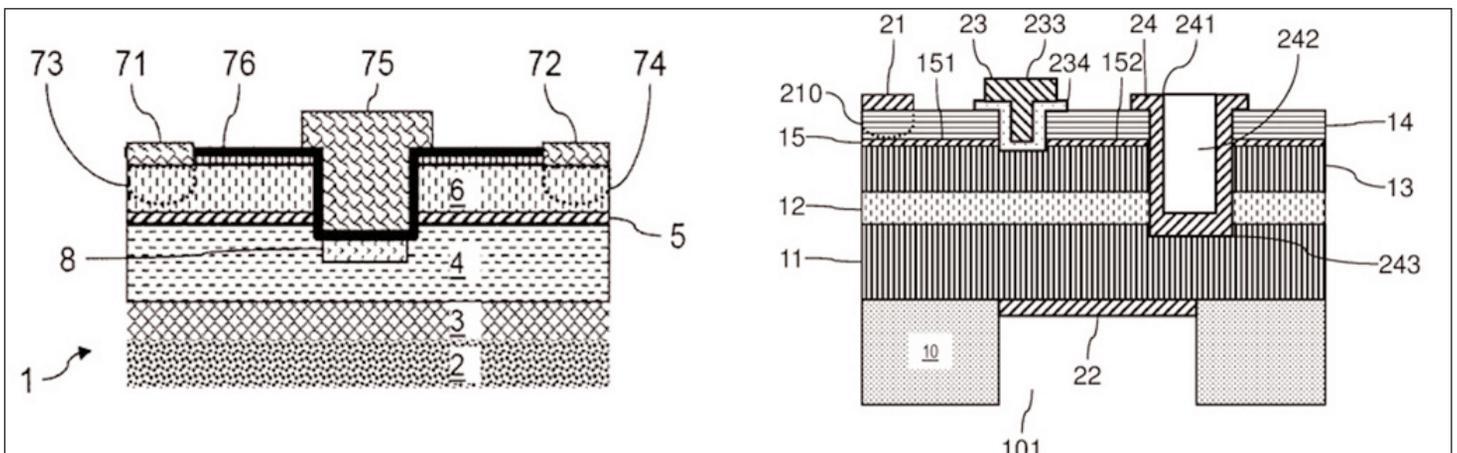
CEA is also a well-established IP player in the GaN-on-Si patent landscape, with more than 40 patented inventions. Over the last three years, it has intensified its GaN-on-Si patenting activity in the field of power applications with six additional inventions. CEA first focused on enhancement-mode device technology (Figure 3a) and then focused on the epi-structures in order to enhance the vertical breakdown voltage. Its recent GaN-on-Si patenting activity also includes an IP collaboration with automotive player Renault regarding power GaN device technology (Figure 3b).

“Following the R&D collaboration between STMicroelectronics and CEA since 2018, and the recent announcement of partnership between STMicroelectronics and TSMC, we expect an acceleration of their respective patenting activity on power GaN-on-silicon in the next months,” says Remi Comyn of Knowmade. ■

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**Figure 3: (a) Method for forming an implanted area under the gate region, for a normally-off heterojunction transistor (US patent 10,164,081). (b) III-N heterojunction transistor with a vertical structure (WO patent application 2018/100262).**