

Positive threshold in GaN transistors with p-type aluminium titanium oxide

An AlTiO gate insulator combined with recessing enables the first demonstration of normally-off, enhancement-mode operation.

The Indian Institute of Science claims the first enhancement-mode (e-mode) operation of aluminium gallium nitride/gallium nitride (AlGaN/GaN) high-electron-mobility transistors (HEMTs) using p-type aluminium titanium oxide (AlTiO) gate insulation [Sayak Dutta Gupta et al, IEEE Transactions on Electron Devices, vol66, issue 6 (June 2019), p2544].

The metal-oxide-semiconductor (MOS) gate stack combined the high-k dielectric properties of TiO₂ (k greater than 60) with the p-type properties supplied by Al₂O₃ doping (k ~9). The Al₂O₃ substitutes the 2Als on Ti sites and the 3Os have a deficit of one vacancy that is doubly positively charged. The charged O vacancy can release two holes, which can subsequently be reabsorbed by uncharged O vacancies. The compensating negative charges on the 2 Al sites are fixed.

The researchers comment: "The ON-state performance of e-mode HEMTs in this paper with p-type AlTiO was found to be on par with the best reports till date."

GaN HEMTs are being developed as power switches, where enhancement-mode as opposed to depletion-mode is desired for low power loss and fail-safe performance. Enhancement-mode devices are in the low-current OFF-state when the gate potential is at 0V. By contrast, depletion-mode operation has the current on with 0V gates and requires a (negative) potential to pinch off the electron flow.

Unfortunately, simple GaN HEMTs are depletion-mode and special extra processing is required to push threshold voltages in a positive direction to give enhancement-mode, normally off performance. The placing of p-type materials, such as magnesium-doped p-GaN, under the gate is one such method for moving to enhancement-mode devices. Recessing the gate into the barrier also pushes the threshold positive, but removing all the barrier material increases on-resistance due to etch damage of the GaN channel surface.

High-k dielectrics give increased electrostatic control of current under the gate with sharper turn-on (low subthreshold swing), while reducing gate leakage, compared with Schottky gate HEMTs.

Metal-organic chemical vapor deposition (MOCVD) on 6-inch (111) silicon substrates produced epitaxial structures with 150nm AlN nucleation, 1µm AlGaIn transition, 3µm GaN buffer/channel, 22nm Al_{0.22}Ga_{0.78}N barrier, and 40nm in situ silicon nitride cap.

Fabricated transistors (Figure 1) consisted of annealed titanium/aluminium/nickel/gold source-drain contacts, plasma-etched mesa isolation, atomic layer etching (ALE) of the AlGaIn barrier for gate recessing, surface treatment and deposition of gate oxide, and nickel/gold gate metal formation and low-temperature annealing.

The gate oxide was applied using BENEQ atomic layer deposition (ALD) equipment. Water (H₂O) was used as

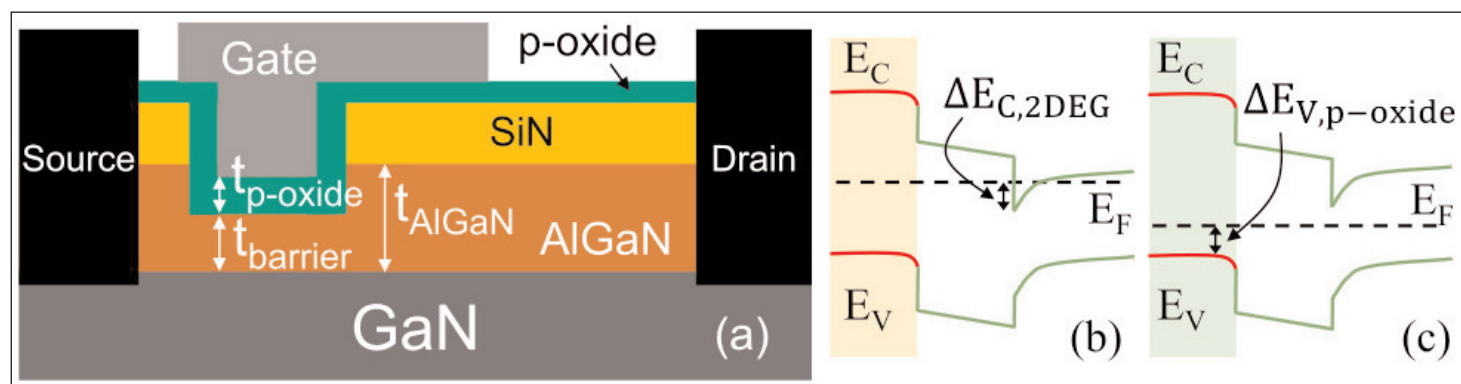


Figure 1. (a) Cross-sectional view of HEMT with p-type metal oxide gate and partially recessed AlGaIn barrier. Energy-band sketch of AlGaIn/GaN HEMTs with (b) conventional dielectric and (c) p-type oxide: p-type oxide shifts Fermi level (E_F) beneath conduction band (E_C) in two-dimensional electron gas (2DEG) channel.

precursor for oxygen in both the TiO_2 and Al_2O_3 components. The titanium was sourced from titanium tetraisopropoxide (TTIP), and aluminium from trimethylaluminium (TMA). The oxide was built up from cycles of Al_2O_3 and TiO_2 layers.

Hall measurements on $\text{Al}_{0.52}\text{Ti}_{0.48}\text{O}$ showed p-type conductivity with a majority hole concentration at $1.4 \times 10^{14}/\text{cm}^3$. The $\text{Al}_{0.52}\text{Ti}_{0.48}\text{O}$ material was compared as a p-type gate oxide against MOS-HEMT structures incorporating pure TiO_2 , sputtered copper oxide or electron-beam evaporated nickel oxide.

Pure TiO_2 gate insulation resulted in depletion-mode operation with a threshold voltage at -4V . With 52% Al in the TiO_2 , the threshold shifted in a positive direction to -0.2V . Post-deposition annealing also pushed the threshold positively as the temperature increased, but the effect became less pronounced for higher Al contents of the AlTiO . The more positive effect at lower contents is due to greater activation of the Al, it is thought. At 52% Al, the number of Ti sites where Al can be activated is limited.

Copper oxide gave a smaller threshold shift than AlTiO . In addition, the gate leakage was increased by up to four orders of magnitude. With nickel oxide, the gate leakage was even worse.

Thinning the barrier by recessing the gate enabled positive threshold voltages to be attained. With the barrier thickness at 8nm , the threshold was $+0.5\text{V}$. The resulting transistor operated in enhancement-mode with the device in the OFF-state at 0V gate potential. The thinner barrier also improved channel control with lower OFF-state current ($100\times$ lower) and improved/lower subthreshold swing at $73\text{mV}/\text{decade}$ (Figure 2).

The threshold voltage hysteresis for drain current–gate voltage dual sweeps was $\sim 30\text{mV}$ and $\sim 40\text{mV}$ with the drain bias at 0.1V and 15V , respectively.

A device with $3\mu\text{m}$ gate length and $17.5\mu\text{m}$ source–drain spacing achieved a drain current $\sim 400\text{mA}/\text{mm}$ at $+4\text{V}$ gate potential. The on-resistance was $8.9\Omega\text{-mm}$, while the on/off current ratio was 10^7 . Gate leakage was less than $200\text{nA}/\text{mm}$.

The OFF-state three-terminal breakdown voltage was more than 600V with the substrate grounded. Catastrophic failure was seen in the mesa isolation, not as usual in the gate–drain region. The researchers expect an increased breakdown voltage from improved mesa isolation processes.

The researchers believe that the threshold can be pushed beyond $+1\text{V}$ with optimization of the p-oxide gate insulation. ■

<https://doi.org/10.1109/TED.2019.2908960>

<https://beneq.com/en>

Author: Mike Cooke is a freelance technology journalist who has worked in the semiconductor and advanced technology sectors since 1997.

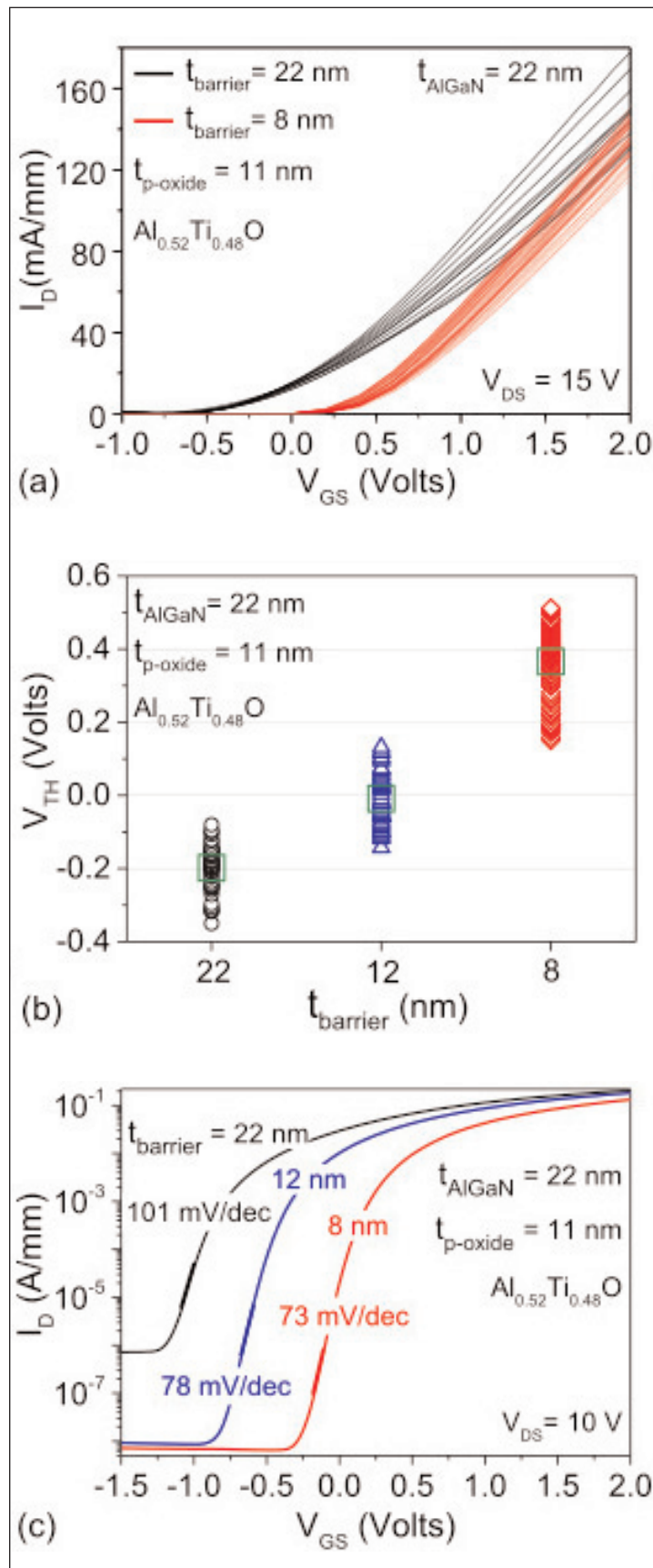


Figure 2. (a) Transfer characteristics of HEMTs with optimized p-oxide and different barrier thicknesses. (b) Shift in threshold (V_{TH}) from negative to positive when barrier thickness under the gate was scaled. (c) Logarithmic plot of transfer characteristics and derived subthreshold swing (SS) values.