# High-current vertical diamond MOSFETs

## Researchers achieve drain currents above 1A by connecting two devices.

**W**aseda University in Japan reports on vertical metal-oxide-semiconductor field-effect transistors (MOSFETs) constructed from diamond with up to 0.7A maximum drain current [Nobutaka Oi et al, IEEE Electron Device Letters, vol.45, issue 9 (September 2024), p1554]. The team claims the 0.7A drain current as the largest reported so far for diamond FETs. Two of the five researchers involved are also affiliated with Japan-based Power Diamond Systems Inc.

Diamond FET devices are potentially a p-type complement for the n-channel devices that are fabricated in silicon carbide (SiC), gallium nitride (GaN) and gallium oxide ($Ga_2O_3$) material systems that are being developed for power electronics applications. Complementary MOSFETs would enable the use of CMOS circuit designs, which enable higher-speed operation and smaller gate drive requirements. In the power domain, efficient complementary inverters are wanted for DC/AC conversion of renewable and stored energy sources.

Diamond material properties suitable for power applications include a high breakdown field (10MV/cm), high thermal conductivity (22W/cm-K), and high hole mobility ($2000–3800cm^2$/V-s).

Two epitaxial diamond layers, 0.5µm undoped and 1.0µm n-type, were added to a 3mmx3mmx0.3mm p++-type boron-doped diamond substrate (Figure 1) by microwave plasma chemical vapor deposition (MPCVD). The carbon came from a mix of methane ($CH_4$) and carbon dioxide ($CO_2$). The n-type nitrogen doping was sourced from nitrogen gas ($N_2$).

The vertical FET structure was fabricated by inductively coupled plasma reactive-ion etch (ICP-RIE), MPCVD diamond regrowth, electron-beam evaporation of the source electrode, plasma treatments for hydrogen termination and device isolation, 450°C atomic layer deposition (ALD) of 200nm aluminium oxide ($Al_2O_3$), tetramethylammonium hydroxide (TMAH) $Al_2O_3$ etch, dual ion beam sputtering of the backside drain contact, and thermal evaporation of the gate and source contact pad.

The ICP-RIE to a depth of 2.2µm created 60µm-wide trenches. The trench length was 5µm. The vertical channel consisted of a two-dimensional hole gas (2DHG) that formed near the interface between the
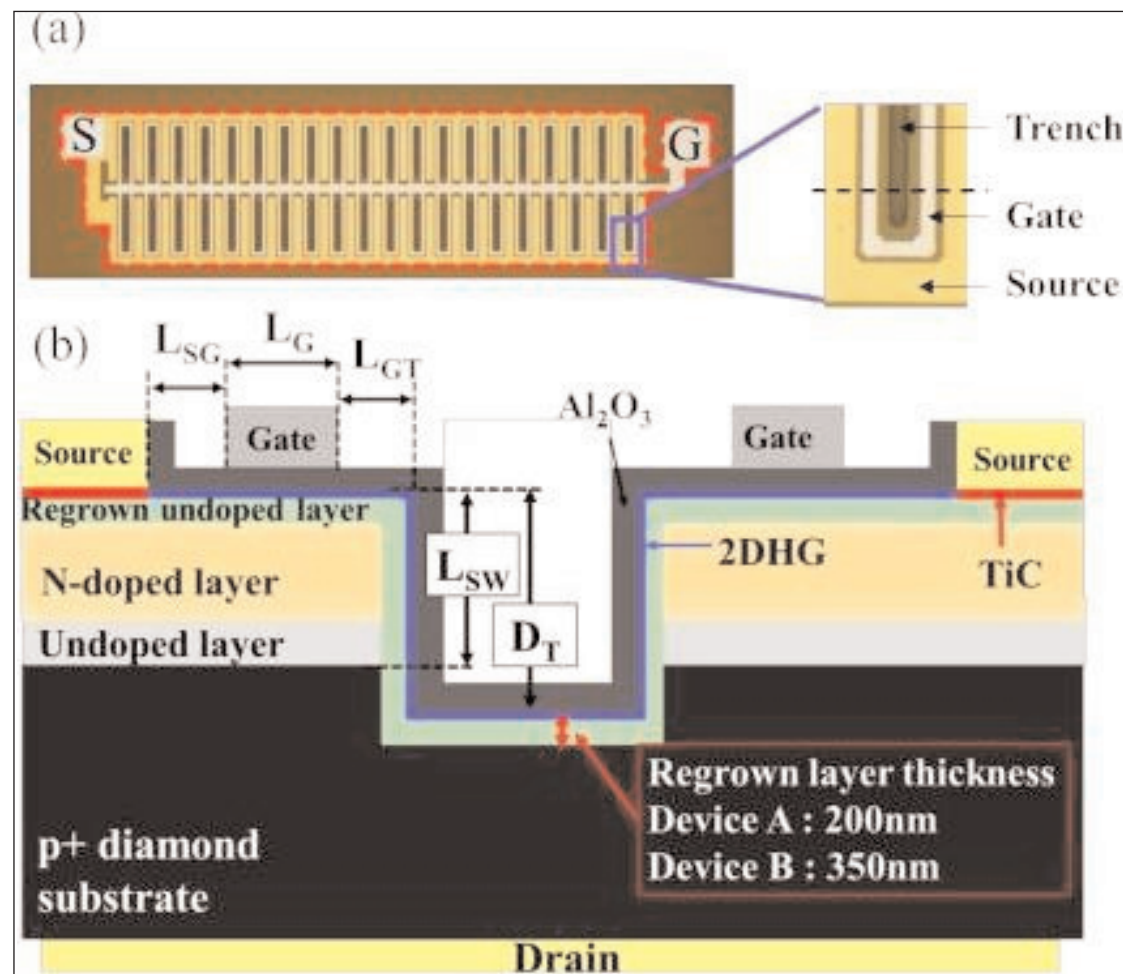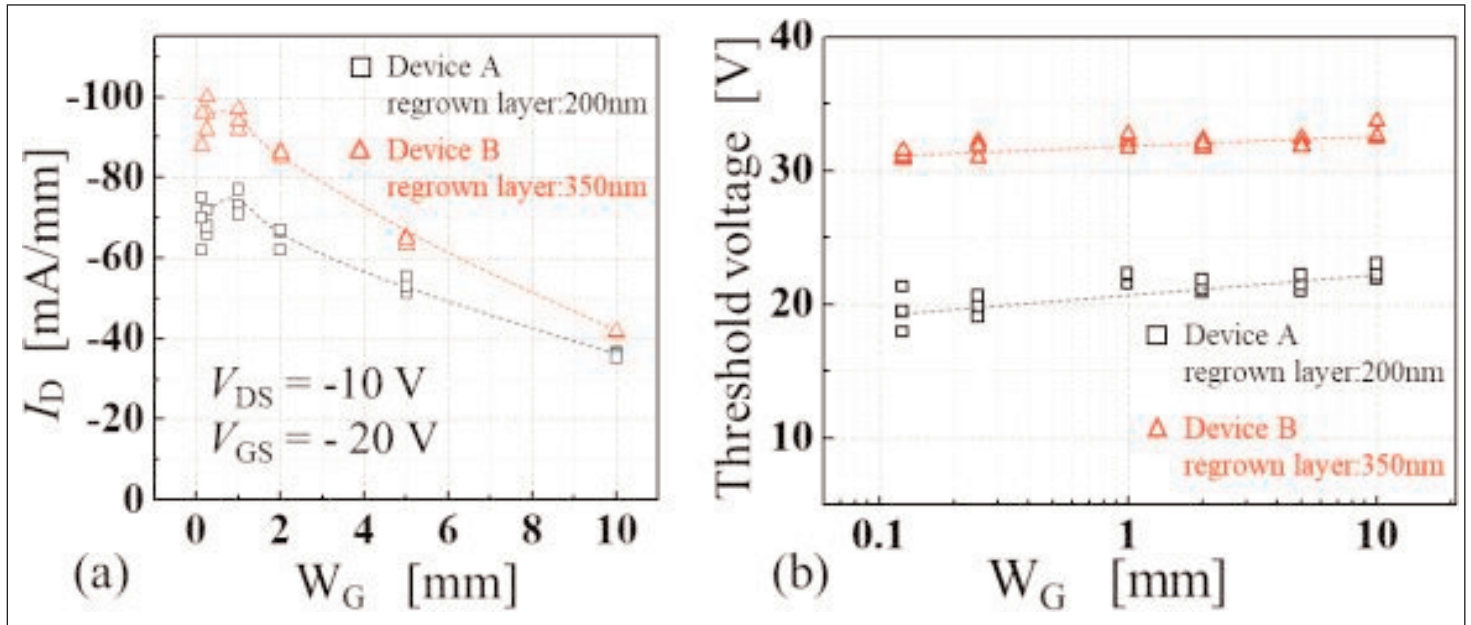


**Figure 1. (a) Optical microscope image and close-up of device with gate width of 5mm (S: source, G: gate) (b) Cross-sectional schematic of dash line area.**

**Figure 2. (a) Drain current density ($I_D$) versus gate width ($W_G$) at −10V $V_{DS}$ and −20V $V_{GS}$. (b) Threshold voltage dependence on gate width.**

regrown diamond and $Al_2O_3$ layers.

The source electrode consisted of titanium/platinum/gold (Ti/Pt/Au), annealed to form titanium carbide (TiC) as the diamond source contact. The drain was Ti/Au. The gate and source pad were Al.

The gate length ($L_G$) was 4μm. The gate widths, the perimeters of the trenches, were varied on a millimeter scale. The distances of the gate from the source ($L_{SG}$) and trench ($L_{GT}$) were 2μm and 3μm, respectively.

A device with 10mm gate width achieved a maximum drain current of −0.7A at −20V drain bias, and −20V gate potential. The regrown layer thickness was

200nm (i.e. device type 'A').

The on/off current ratio was around 9.5 orders of magnitude with the off-current reaching down to the measurement limit of the team's equipment (~$10^{-11}$A) when the gate was at 35V.

With a −1V drain bias, the threshold voltage was +21.2V, so the device operated in a normally-on (when the gate potential is 0V) depletion mode. For many power applications, a normally-off mode is preferred.

Another device A, with 0.1mm gate width, achieved an off-state (+30V $V_{GS}$) breakdown voltage of 225V. The drain current was less than $10^{-10}$A almost up to
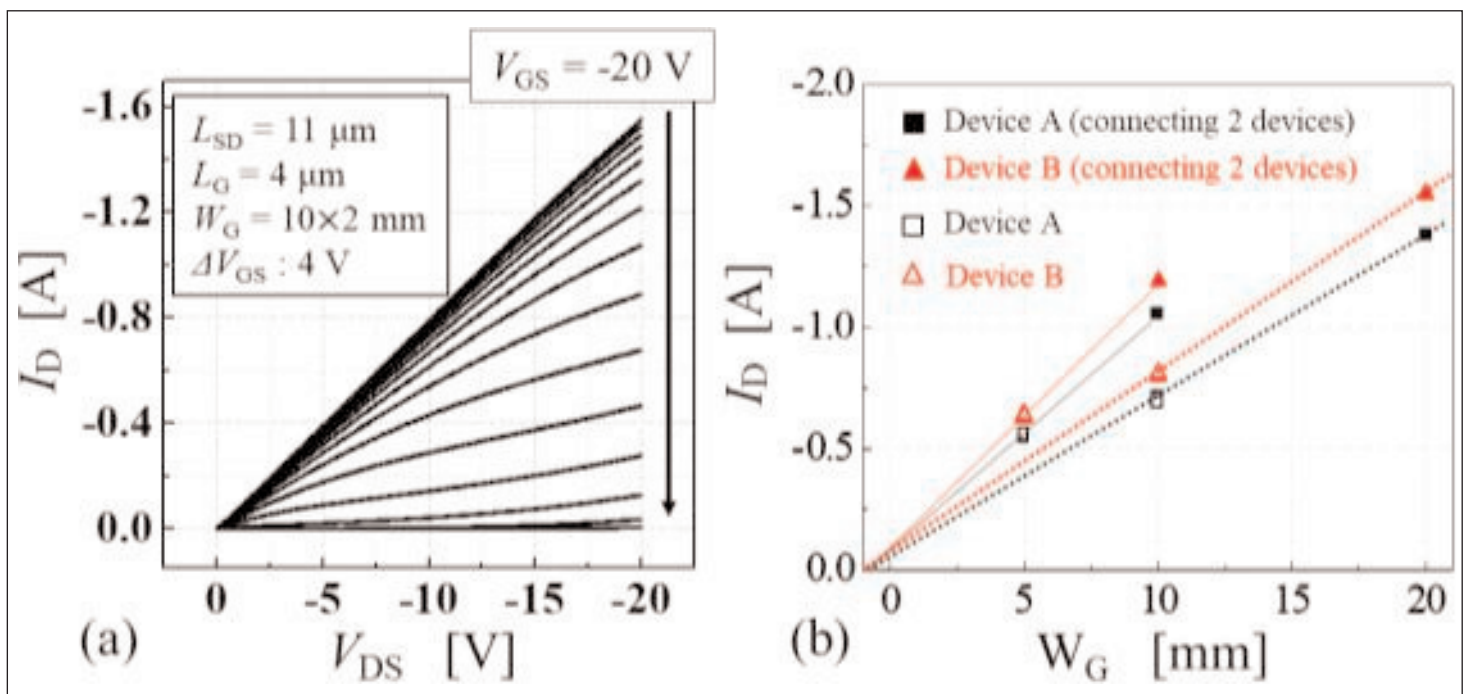


**Figure 3. (a) $I_D$–$V_{DS}$ pulse mode characteristics of two connected B devices with $V_{GS}$ ranging from −20V to +36V. (b) Relationship between drain currents of single and double devices at −20V $V_{DS}$ and −20V $V_{GS}$.**

the breakdown point.

The team comments: "Breakdown voltage is expected to be lower for devices of larger gate width because of inhomogeneous distribution of device characteristics due to process non-uniformity."

The drain current density normalized by the gate width tended to fall for the wider devices (Figure 2). Also, a thicker 350nm ('B') regrown layer gave around 30% higher drain current for the 1mm-wide FETs tested.

The researchers comment: "The tendency for the drain current density to decrease as WG increases suggests the presence of additional resistances such as substrate resistance and source electrode resistance, with the latter expected to play a more significant role."

For devices wider than 2mm, the measurements were made in pulse mode to avoid self-heating effects.

The threshold voltages were larger for the B series, meaning that they were deeper into depletion-mode territory. The specific on-resistances were $48.4m\Omega\text{-cm}^2$ and $36.7m\Omega\text{-cm}^2$ for 2mm WG devices A and B, respectively. These values were reduced by subtracting the effect of the source electrode area from the total active area to $17.7m\Omega\text{-cm}^2$ and $13.8m\Omega\text{-cm}^2$, respectively. The team suggests that the electrode contact resistance could be improved through use of an interlayer dielectric and reduction of device dimensions.

To achieve more than 1A drain current, the researchers connected two devices (Figure 3). For 10mm wide device B, two devices enabled –1.5A to be reached with an on-resistance of $12.7\Omega$, just over half the value for a single FET. The maximum drain current for type A was –1.3A. ∎

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