ETRI develops p-type selenium-tellurium alloy transistor

South Korea's Electronics and Telecommunications Research Institute shows how it is possible to overcome the low mobility of p-type semiconductors while improving display refresh rates and power consumption.

South Korea's non-profit, government-funded Electronics and Telecommunications Research Institute (ETRI) has developed a p-type Se–Te (selenium–tellurium) alloy transistor that can be easily deposited at room temperature via a simple process using a chalcogenide-based p-type semiconductor material. In addition, they have also developed a new technology that can systematically adjust and control the threshold voltage of n-type transistors through charge injection control of Te thin films in the hetero-junction structure of n-type oxide semiconductor and p-type Te (Kyunghee Choi et al, ACS Applied Materials & Interfaces, vol. 16, issue 18, p23459).

One of the most widely used materials in the current display industry is the indium gallium zinc oxide (IGZO)-based n-type oxide semiconductor. In the case of p-type semiconductors, p-type LTPS (low-temperature polycrystalline silicon) is used due to the lack of processability and electrical properties compared to n-type oxide semiconductors, but there has always been many limitations in that it is much more expensive to manufacture and the size of the substrate is limited.

However, with the increase in demand for higher refresh rates (240Hz+) in high-resolution displays, especially at SHV-class resolution displays (8K-4K), interest in the development of p-type semiconductors has reached its peak in recent years. Since n-type semiconductor-based transistors, which have been used in existing displays, have limitations in effectively implementing displays with high refresh rates, demand for p-type semiconductors is rising rapidly.

To meet these needs, ETRI developed a p-type semi-conductor by adding Te to Se, increasing the crystal-lization temperature of the channel layer, depositing an amorphous thin film at room temperature and crystal-lizing it through a subsequent heat treatment process. As a result, they have improved mobility and achieved a higher level of on/offline current ratio characteristics compared with existing transistors.

The researchers have also confirmed that, when a Te-based p-type semiconductor was introduced as a heterojunction structure over an n-type oxide semi-conductor thin film, the threshold voltage of the n-type transistor can be adjusted by controlling the flow of electrons within the n-type transistor, depending on the thickness of Te. In particular, they have improved the stability of the n-type transistor without the need of a passivation layer, by adjusting the thickness of Te in the heterojunction structure.

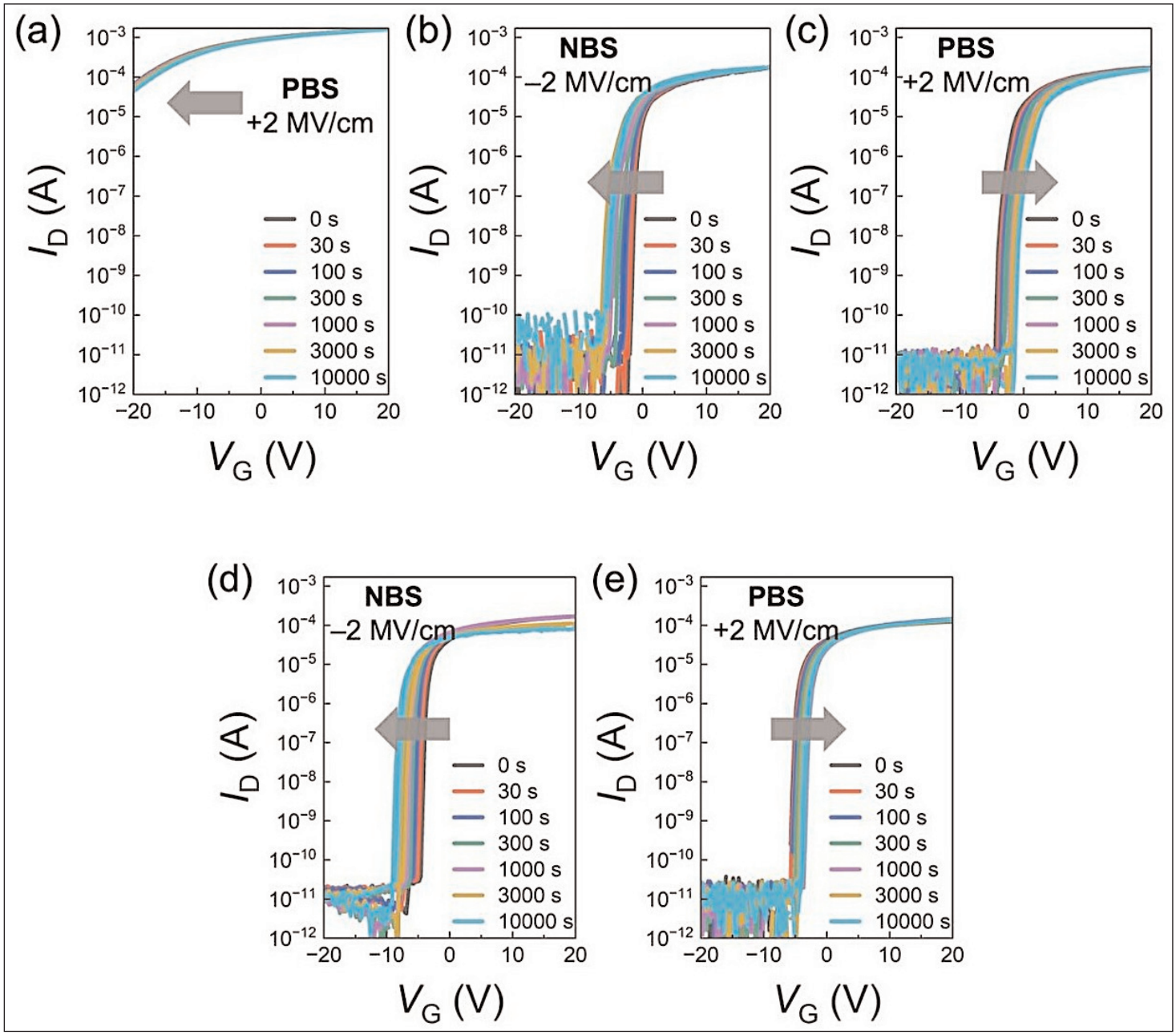
By utilizing these achievements, it is expected that the growth of the next-gen display industry will reach new heights, enabling the development of new displays with better resolution and lower power consumption at the same time.

In fact, this new discovery can also impact the semi-conductor industry. Currently, many leading global semiconductor manufacturers are focusing on the development of new scale-down processes that can increase the integration of their products but, according to the analysis of many industry insiders, the level of integration in semiconductors has reached its limit.

Accordingly, in recent years, new integration methods have been introduced to stack multiple semiconductor chips at once. Among them, TSV (through-silicon vias) is the most well known, where multiple wafers are stacked and a hole is drilled into the wafers to ensure electrical connection. The TSV method has the advantage of effective utilization of space and reduced power consumption. However, there are still many limitations that need to be addressed, including high processing costs, low yield, etc.

To overcome the limitations of TSV, the industry has come up with monolithic 3-dimensional (M3D) integration, where the materials are stacked onto a single wafer instead of stacking multiple layers at once. Unfortunately, the M3D method has not yet reached commercialization due to various issues such as the limited use of high-temperature processes, etc.

However, many experts consider that the hetero-junction thin-film transistor and p-type semiconductor device developed by ETRI can operate stably even in processes below 300_, pushing the industry a step



Transfer curves of the (a) Al:IZTO under PBS of +2 MV/cm for 10,000 s before passivation, single Te heterojunction TFTs with passivation under (b) NBS and (c) PBS, double Te heterojunction TFTs under (d) NBS and (e) PBS of V_D = 1 V, –2 MV/cm and +2 MV/cm for 10,000 s.
Graphic courtesy of: ACS Applied Materials & Interfaces (2024). DOI: 10.1021/acsami.4c02681.

closer to the commercialization of M3D.

"This is a monumental achievement that can be widely utilized in next-gen displays such as OLED TVs and XR devices, as well as future researches in other fields such as CMOS (complementary metal oxide semiconductor) circuits and DRAM memories," says Cho Sung-Haeng, principal researcher of ETRI's Flexible Electronics Research Section.

Researchers of ETRI say that they are planning to optimize the Te-based p-type semiconductors to large-sized substrates of 6-inches or more and to secure its potential for commercialization by applying them to various circuits, ultimately finding new ways to implement them into new fields.

The research was carried out as a part of the National Research Council of Science and Technology's Creative Convergence Research Project 'M3D Oxide Semiconductor-Based Ultra-Low Power, High-Band, Large-Capacity DRAM Development', the Ministry of Trade, Industry and Energy's Industrial Technology Challenge Track 'TFT for the Development of a Non-Silicon Semiconductor for High-Resolution & Large-Sized Displays and Core Technologies for CMOS Manufacturing', and ETRI's Research Project for the Next Generation 'Development of High-Performance Semiconductor Transistors for Ultra-Low Power Multi-Value Devices'. ■

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