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COMPOUNDS & ADVANCED SILICON

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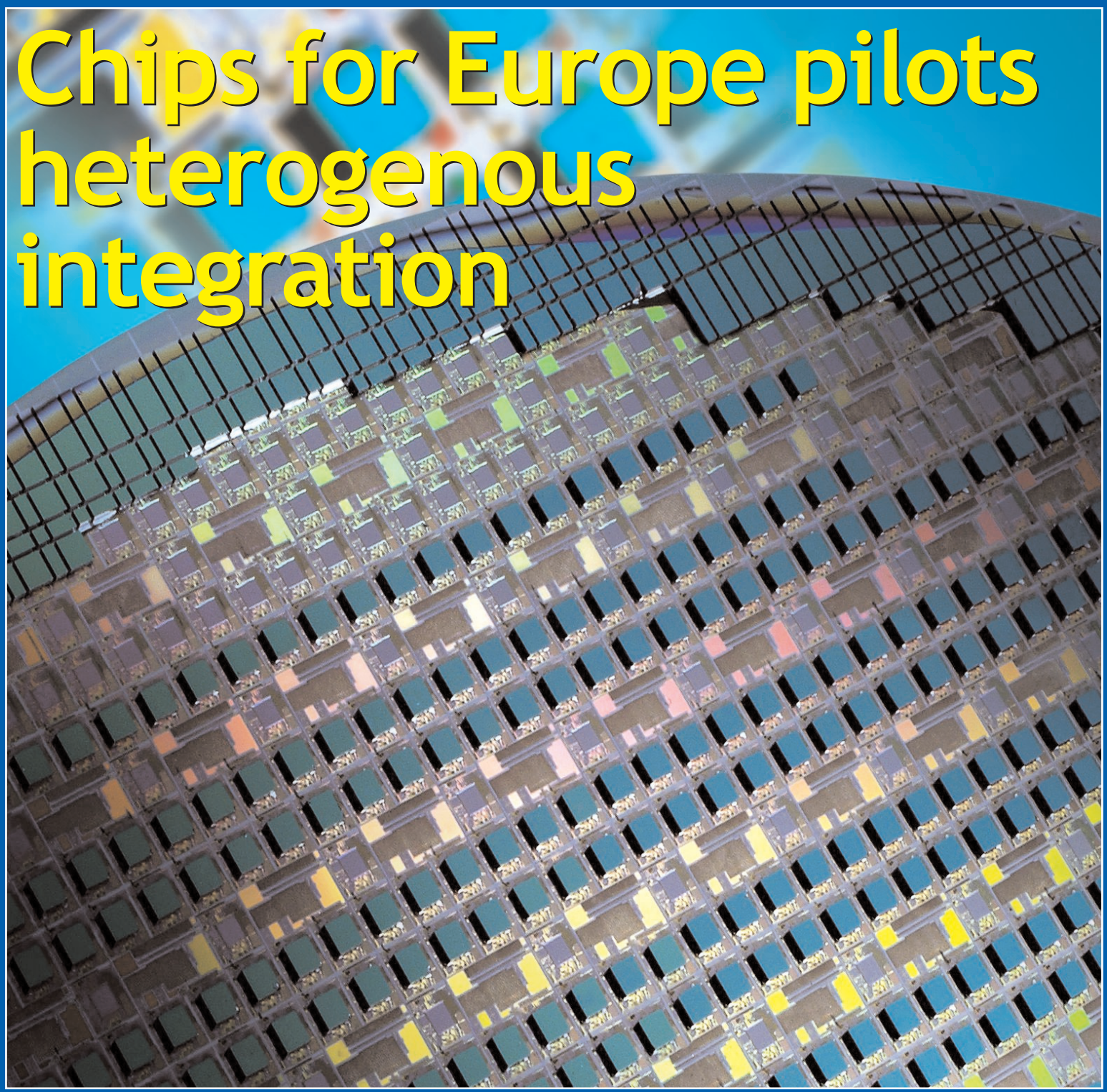

Chips for Europe pilots heterogenous integration

Indichip to build $1.4bn SiC fab • CHIPS Act funding for MACOM
METLEN to produce gallium in Greece • Thorlabs buys Praevium

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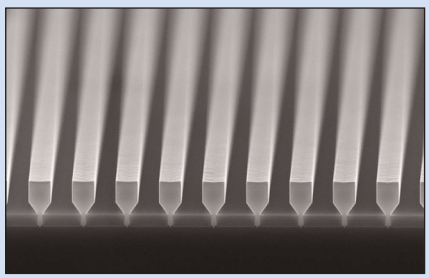
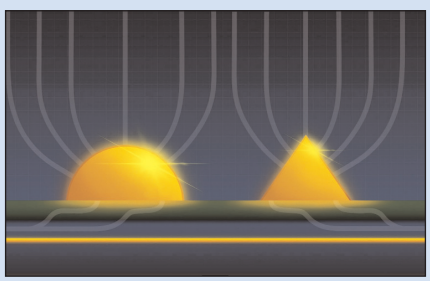
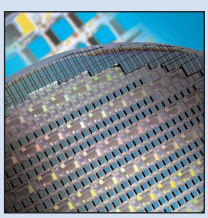
p22 The Vermont Gallium Nitride Tech Hub has been awarded $23.7m in federal funding from the US Economic Development Administration.



p46 GaAs-based nano-ridge array after epitaxy, monolithically fabricated on 300mm silicon wafers in imec's CMOS pilot prototyping line.



p47 CAD software developer Photon Design has previewed its quantum dot module added to its laser simulator.



Cover image: Post-CMOS pressure sensor chiplets with wafer level packaging before dicing, courtesy of Germany's Fraunhofer ISIT. The APECS (Advanced Packaging and Heterogeneous Integration for Electronic Components and Systems) pilot line has begun operation. **p9**

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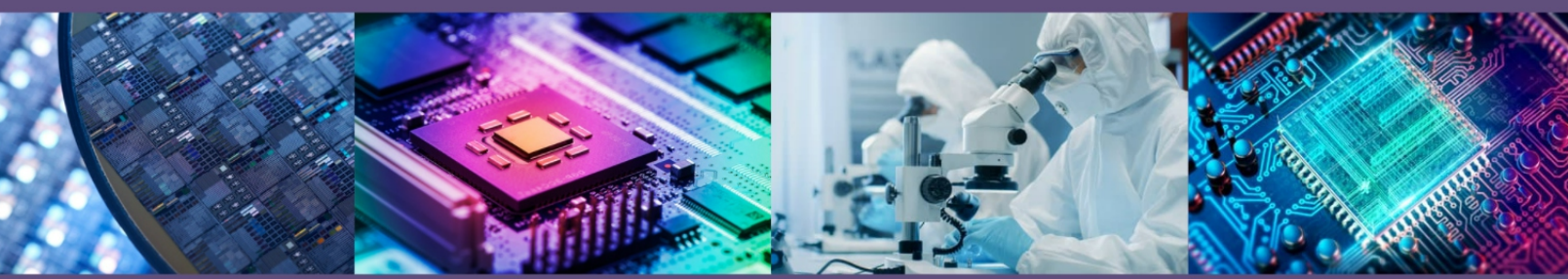

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Micro-LED display market to grow to 34.6 million by 2031

Forecast reduced after Apple postponed project for watch in early 2024

Shipments of micro light-emitting diode (LED) displays will surge to 34.6 million units by 2031, according to the 'Micro LED Display Market Tracker – 4Q 2024' of market research firm Omdia. However, despite this growth, micro LED displays are expected to account for just 0.9% of the total display market, as the technology remains competitive only in select applications over the forecast period.

Following reports in February 2024 that Apple postponed its micro-LED display project for its watch, some set brands and related suppliers have slowed their development of associated components and equipment. As a result, Omdia has significantly revised its market forecast compared with projections made earlier in 2024.

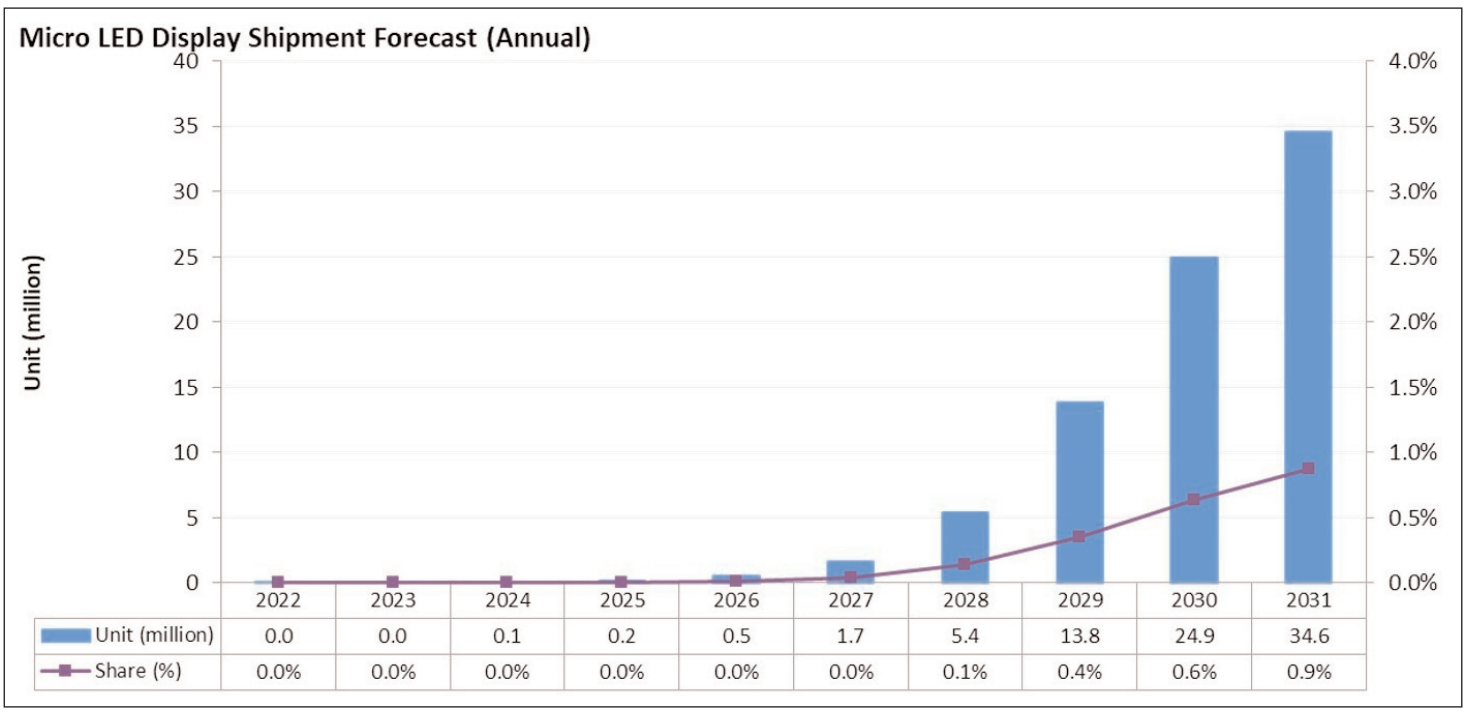
Despite some delays, many industry players continue to aggressively develop micro-LED display technology. Omdia forecasts that shipments in the micro-LED display market will reach 1.7 million by 2027, driven primarily by light-emitting diode-on-silicon backplane (LEDoS) in ultra-small-sized display devices such as extended reality (XR) devices, particularly smart glasses designed for outdoors. By 2031, XR devices are expected to account for 24.4% of the micro-LED display market.

"Smart-glasses require light-weight designs, low power consumption and high readability under sunlight," says senior research manager Jerry Kang. "A few LEDoS suppliers have already achieved diagonal sizes as small as 0.15-inch, making them more suitable for lightweight on smart glasses compared to other display technologies," he adds.

In 2024, numerous display manufacturers unveiled new micro-LED display prototypes that mainly targeted automotive, public displays, and virtual studios. This trend suggests that suppliers are anticipating greater adoption of micro-LED displays in niche applications.

"Due to the low cost competitiveness, many display suppliers are focusing on penetrating product segments where OLED or LCD struggle to meet customer demands for specific display sizes and performance," says Kang. "Simultaneously, several component and equipment suppliers are proactively introducing advanced technologies to enhance the manufacturing of micro-LED displays."

https://omdia.tech.informa.com/collections/afccd050/micro-led-display-market-tracker



	2022	2023	2024	2025	2026	2027	2028	2029	2030	2031
Unit (million)	0.0	0.0	0.1	0.2	0.5	1.7	5.4	13.8	24.9	34.6
Share (%)	0.0%	0.0%	0.0%	0.0%	0.0%	0.0%	0.1%	0.4%	0.6%	0.9%

Silicon PIC market growing at 45% CAGR from $95m in 2023 to $863m in 2029

Future of high-speed optical communication lies in SOI, LNOI and InP material platforms

Silicon photonics continues to evolve rapidly, with diverse applications signaling significant opportunities ahead, notes market analyst firm Yole Group. Specifically, the market for silicon photonic integrated circuit (PIC) die is estimated to be increasing at a compound annual growth rate (CAGR) of 45% from 2023 to at least $863m by 2029, notes the firm in its annual report 'Silicon Photonics 2024 — Focus on SOI [silicon-on-insulator], SiN [silicon nitride], and LNOI [lithium niobate-on-insulator] platforms', which this year explores the photonics landscape, emphasizing materials for PICs, optical interconnects, and other applications.

While silicon photonics plays a pivotal role in the semiconductor industry and is widely used in communication and sensing applications, the photonics market remains challenging for both established players and new entrants, notes Yole. Over the next decade, Yole expects key players to emerge, driving industry consolidation. However, the wide range of use cases will provide ample room for growth and innovation.

"This growth will be driven mainly by high-data-rate pluggable modules for increased fiber-optic network capacity," says Martin Vallo, senior technology & market analyst, Photonics, at Yole Group. "Additionally, projections of rapidly growing training data-set sizes show that data will need to use light for scaling machine learning (ML) models, using optical I/O in ML servers."

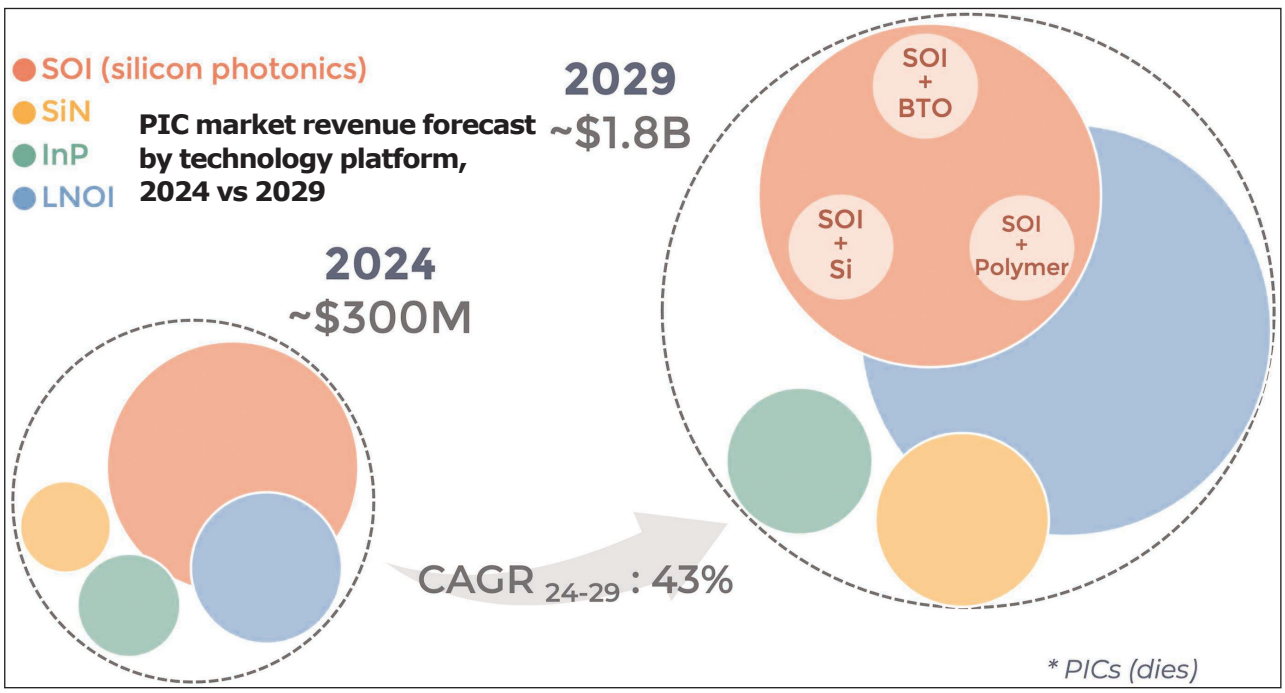
Data centers are the primary application for silicon photonics, with new Chinese leaders emerging daily. Telecoms is another key area that leverages silicon's superior performance. Optical LiDAR systems also show promise but face cost and beam-scanning hurdles, notes Yole.

In healthcare, advanced photonic components could revolutionize diagnostics, treatment, and monitoring, though regulatory challenges must be addressed. Silicon photonics holds strong potential across these fields, it is reckoned.

This year's report provides an analysis of data-center networks (with detailed market forecasts between 2023 and 2029 for datacom, telecom, and sensing applications), and examines the supply chain and market shares of the datacom and telecom sectors. A special focus on technologies and innovations addresses challenges in CMOS-foundry-compatible devices, circuits, integration, and packaging. There is also a dedicated chapter on the Chinese photonics ecosystem. China has made notable strides in silicon photonics and is aiming for global leadership, notes Yole.

The 2024 report highlights key technologies shaping the photonics landscape, including LNOI/TFLN (lithium niobate-on-insulator/thin-film lithium niobate) and InP (indium phosphide). "For instance, the LNOI market is projected to reach nearly $1bn by 2029, with an impressive 98% CAGR," says Eric Mounier, chief analyst, Photonics & Sensing, at Yole Group. "TFLN and LNOI stand out for their low optical loss and high bandwidth. The InP PIC market is expected to grow at a 22% CAGR, while the SiN segment shows strong potential with a 43% CAGR during the same period."

www.yolegroup.com



Fraunhofer IAF gains €4.35m from Baden-Württemberg to contribute to EU Chips Act-funded APECS pilot line

New epi, process and metrology equipment to produce chiplets and interposers on 6" wafers

The Fraunhofer Institute for Applied Solid State Physics IAF of Freiburg, Germany says that, as part of the pilot line 'Advanced Packaging and Heterogeneous Integration for Electronic Components and Systems' (APECS), it will continue to expand its semiconductor research infrastructure in the coming years, supported by national funding of €4.35m via the state of Baden-Württemberg. A cheque was symbolically handed over in a visit on 16 December by Dr Patrick Rapp, the Minister for Economic Affairs, Labour and Tourism.

State Secretary Dr Patrick Rapp, Ministry of Economic Affairs, Labour and Tourism, hands over the symbolic cheque for €4.35m to Dr Patricie Merkert and professor Rüdiger Quay of Fraunhofer IAF. (photo © Fraunhofer IAF).

Also, Rapp was informed about the planned measures and the APECS pilot line, which will be coordinated by the Fraunhofer-Gesellschaft and implemented by the Research Fab Microelectronics Germany (FMD) over the next 4.5 years. APECS will make it possible to further expand the R&D infrastructure across Europe. Total funding of €730m is provided by Chips Joint Undertaking, Germany's Federal Ministry of Education and Research (BMBF) and other funding.

"The APECS pilot line is a project of strategic importance for Baden-Württemberg, as it is about participating in highly innovative developments in the field of semiconductor technologies and supporting a rapid transfer to our companies," said Rapp.

APECS: Heterogeneously integrated technologies

The APECS pilot line is an important component of the EU Chips Act to drive chiplet innovation and increase research and manufacturing capacity for semiconductors in Europe. The institutes cooperating in the FMD are working closely with other European partners to set up the pilot line and are thus helping to strengthen Europe's technological resilience and boost global competitiveness in the semiconductor industry.

As part of the APECS pilot line, the dry etching technology area in the Fraunhofer IAF cleanroom for 6" wafers is being expanded. (photo © Fraunhofer IAF).

The pilot line will provide large industrial companies as well as small- and medium-sized enterprises (SMEs) and start-ups with low-threshold access to cutting-edge technologies and ensure secure, resilient semiconductor value chains. APECS is co-funded by Chips Joint Undertaking and by national funding from Austria, Belgium, Finland, France, Germany, Greece, Portugal and Spain under the Chips for Europe initiative. Total funding for the APECS pilot line is €730m over 4.5 years.

The APECS pilot line focuses on the scalable industrial transfer of newly developed innovations in heterointegration, in particular the use of new chiplet technologies, thus building a bridge to application-oriented research. APECS goes beyond conventional system-in-package (SiP) methods and aims to deliver robust and trustworthy heterogeneous systems that significantly increase the innovative capacity of the European semiconductor industry.

Chiplets for high-frequency applications and production on 6" wafers

As an institute cooperating in the FMD, Fraunhofer IAF is developing novel chiplets based on the hybrid material systems indium gallium arsenide-on-silicon (InGaAs-on-Si) and gallium nitride-on-silicon carbide (GaN-on-SiC) as well as micro-bump interposers as part of APECS. These technologies are particularly suitable for high-frequency applications due to their outstanding values in key parameters such as noise, output power and efficiency and promise innovations in measurement technology, communication, radar technology and sensor technology.

"Chiplets offer significant advantages in the development and production of high-performance electronic and optical components, as they enable compact and highly efficient multi-functional systems," says Dr Patrick Waltereit, head of Fraunhofer IAF's Technology department. "The combination of different functions such as control logic and amplifiers on one carrier improves both the performance and energy efficiency of a system."

To ensure easy transfer to industry, the development and production of the chiplets and interposers at Fraunhofer IAF will take place on 6" wafers. New equipment for epitaxy, process technology and metrology will therefore be procured and put into operation in the institute's cleanroom. In addition, existing processes for chiplet and interposer production are being adapted.

www.apecs.eu

APECS pilot line starts operation

Advanced Packaging and Heterogeneous Integration for Electronic Components and Systems joins other EU Chips Act-funded pilot lines

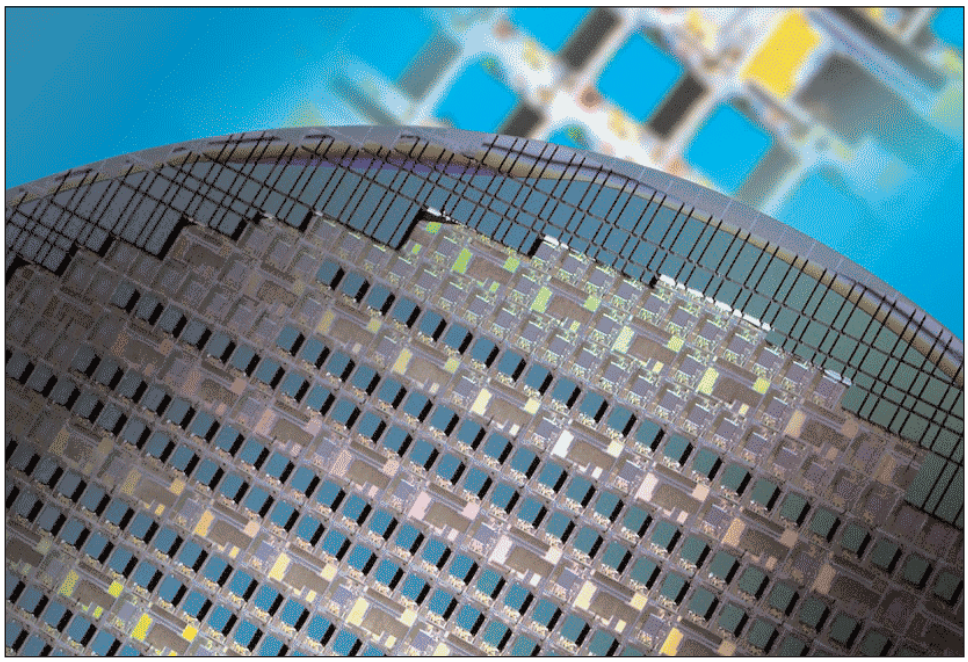
Within the framework of the EU Chips Act, the APECS pilot line has begun operation, providing large industry players, SMEs and start-ups with access to cutting-edge technology for 'Advanced Packaging and Heterogeneous Integration for Electronic Components and Systems' as it aims to establish a foundation for resilient and robust European semiconductor supply chains.

Total funding of €730m over 4.5 years comes from the Chips Joint Undertaking and the funding authorities of the nations involved, through the 'Chips for Europe' initiative. Specifically, the APECS consortium gathers the technological competences, infrastructure and expertise of ten partners from eight European countries:

- Germany (Fraunhofer-Gesellschaft as coordinator, FBH, IHP),
- Austria (TU Graz),
- Finland (VTT),
- Belgium (imec),
- France (CEA-Leti),
- Greece (FORTH),
- Spain (IMB-CNM, CSIC) and
- Portugal (INL).

APECS is implemented by the Research Fab Microelectronics Germany (FMD). Within APECS, the institutes collaborating in FMD will work closely with European partners, to contribute to the European Union´s goals of increasing technological resilience, strengthening cross-border collaboration and enhancing global competitiveness in semiconductor technologies.

The APECS pilot line focuses on bridging application-oriented research with innovative developments in heterogeneous integration, in particular emerging chiplet technologies. By pushing beyond conventional system-in-package (SiP) methods, APECS aims to deliver robust and trusted heterogeneous systems, boosting the innovation capacity of the European semiconductor industry.



Post-CMOS pressure sensor chiplets with wafer level packaging before dicing. © Fraunhofer ISIT.

Due to substantial funding from Germany's Federal Ministry of Education and Research (BMBF) and the federal states of Saxony, Berlin, Bavaria, Schleswig-Holstein, Baden-Württemberg, North Rhine-Westphalia, Brandenburg, and Saxony-Anhalt, it will be possible to further expand the R&D infrastructure in the coming years within the framework of the APECS pilot line.

"APECS is an example how to connect research with business — it underscores how close cooperation with ministries and other partners can secure Europe´s position in the global microelectronics market," says Fraunhofer-Gesellschaft's president professor Holger Hanselka.

Single point of contact to APEC

The APECS pilot line aims to play a key role in supporting European microelectronics by developing new system integration technologies and unlocking new functionalities within the system-technology co-optimization (STCO) approach. This should enable European firms to develop advanced products, even in low quantities, at competitive costs. By providing a wide range of technologies on a single platform, APECS is placed to be Europe's leading hub for developing advanced packaging and heterogeneous integration.

As a cooperation of the Fraunhofer Group for Microelectronics with the Leibniz institutes FBH (Ferdinand-Braun-Institut) and IHP (Institute for High Performance Microelectronics), the Research Fab Microelectronics Germany (FMD) is the central contact for all matters concerning micro- and nanoelectronics. As a one-stop shop, FMD has been combining scientific excellence, application-oriented technologies and system solutions of the 13 cooperating institutes from the Fraunhofer-Gesellschaft and Leibniz Association into a broad customer-tailored technology portfolio since 2017.

Users should benefit from a single point of contact to the APECS pilot line, since it will cover end-to-end design and pilot production capabilities and accelerate progress from cutting-edge research to practical, scalable manufacturing solutions.

Boosting innovation through multi-level collaboration

The APECS pilot line builds on structures established by FMD. In Germany, 12 institutes from the Fraunhofer Group for Microelectronics and the two Leibniz institutes FBH and IHP participate in APECS. The work is led by the central office in Berlin.

"For years, the FMD has successfully combined the strengths of decentralized research institutions with the collaborative potential of a centralized microelectronics hub. This illustrates how APECS is set to become a long-term accessible pilot line for all European stakeholders across the entire value chain," says professor Albert Heuberger, spokesman of the Fraunhofer Group for Microelectronics and chairman of the FMD. "Together with the other EU Chips Act pilot lines, APECS will be a crucial component for heterogeneous integration and advanced packaging of the envisioned pan-European pilot line facility — and thus an indispensable instrument of EU Chips Act."

Semiconductor R&D is at the core of current technological (r)evolutions, ranging from artificial intelligence and high-performance computing, modern defense systems to robotics, power electronics, wireless communication, e-healthcare, quantum technologies, and more. Such future electronic systems will require more and more functions that cannot be provided by a single chip, even if advanced system-on-chip (SoC) concepts are used. Heterogeneous integration will go beyond existing system-in-package (SiP) approaches. This concept of true heterogeneous integration is extremely important for next-generation devices based on future CMOS nodes, silicon germanium (SiGe), silicon carbide (SiC), III/Vs such as gallium arsenide (GaAs) or gallium nitride (GaN) and all different types of microelectro-mechanical systems (MEMS).

Intellectual property (IP) blocks made in different technology nodes will be combined on an active interposer to reduce cost by increasing the production yield (smaller chips) and reuse across applications. This will also touch upon environmental properties of electronics in terms of resource efficiency, critical raw materials, modularity and re-usability of design blocks.

www.forschungsfabrik-mikroelektronik.de/en.html
www.apecs.eu

Altum RF wins two-year ESA contract to supply Ka-band MMIC power amplifiers

Altum RF of Eindhoven, The Netherlands (which designs RF, microwave and millimeter-wave semiconductors) has announced a two-year contract with the European Space Agency (ESA) under the ARTES (Advanced Research in Telecommunications Systems) Core Competitiveness (CC) Programme, for designing and developing high-efficiency monolithic microwave integrated circuit (MMIC) power amplifiers, which will be tailored for phased-array Ka-band satellite communication systems in space applications. The Netherlands Space Office (NSO) was instrumental in facilitating the contract.

Commencing in October, the project aims to advance the development of high-efficiency MMIC power amplifiers to enhance the performance of Ka-band phased-array satcoms systems. With the rapid deployment of low Earth orbit (LEO), medium Earth orbit (MEO) and geostationary orbit (GEO) satellite constellations, Ka-band phased-array systems will play a critical role in future satellite communications. To meet the increasing demand for improved performance in these systems, the project will implement an innovative approach to power amplifier design, delivering significant improvements in both power efficiency and RF performance.

The development project with ESA aligns with Altum RF's strategic vision and product roadmap, says CEO Greg Baker." Over the next two years, this contract will help direct our product development and accelerate our growth in the SATCOM market. The collaboration with ESA during our initial contract was very successful and we look forward to building on that relationship with a continued focus on innovative satellite-based solutions," he adds.

"ESA has been an exceptional partner in helping Altum RF establish itself within the European and global market," comments Niels Kramer, managing director Europe & VP marketing. "This new contract enables us to further expand our design and development capabilities at our Eindhoven office, positioning us to capitalize on this growing business opportunity," he adds.

"By supporting the development of high-efficiency amplifiers, ARTES CC aims at bringing innovation in satellite communications and strengthening industrial competitiveness," notes Domenico Mignolo, ESA's head of Technology and Products Division.

Altum RF designs high-performance RF to millimeter-wave semiconductor solutions for next-generation markets and applications. Collaborating closely with customers and partners, we provide comprehensive technical support and customer service. Our global partnerships enable us to manage the entire product development cycle, from design to packaging, testing, and qualification, significantly reducing time to market.

https://connectivity.esa.int/core-competitiveness
www.altumrf.com

DOE announces $179m funding for Microelectronics Science Research Centers

Focus on basic research to transform the energy efficiency of microelectronics and create microelectronics for extreme environments

The US Department of Energy (DOE) has announced $179m in funding for three Microelectronics Science Research Centers (MSRCs), which will perform basic research in microelectronics materials, device and system design, and manufacturing science to transform future microelectronics technologies.

The MSRCs were authorized by the Micro Act, passed in the CHIPS and Science Act of 2022, and complement the activities appropriated under the CHIPS and Science Act at the Department of Commerce, the Department of Defense, and other agencies.

The DOE notes that, beyond Moore's Law, the emergence of new computing, artificial intelligence and sensing workloads, in addition to rapidly expanding data, have resulted in an unprecedented need and opportunity to redesign the microelectronics materials and innovation process. In addition to needing more energy-efficient microelectronics, DOE also needs microelectronics designed to operate in extreme environments, including high-radiation, cryogenic, and high-magnetic-field environments.

"Advancements in microelectronics are critical to furthering scientific discovery," says Harriet Kung, who is Department of Energy's Office of Science Deputy Director for Science Programs. "The innovations that come from these research centers will improve our daily lives and drive forward US leadership in science and technology."

The three MSRCs are:

- **The Microelectronics Energy Efficiency Research Center for Advanced Technologies (MEERCAT)**

MEERCAT aims to advance integrated innovations across materials, devices, information-carrying modalities, and systems' architectures. Focusing on intelligent sensing, data bandwidth, multiplexing, and advanced computing, the center will explore transformative solutions that seamlessly bridge sensing, edge processing, artificial intelligence, and high-performance computing. Through end-to-end co-design, spanning nanoscale materials, neuromorphic architectures, in-transit data processing, and heterogeneous integration, MEERCAT aims to discover new approaches for real-time energy-efficient information handling. By leveraging state-of-the-art methods for synthesis, simulation and prototyping, the center will accelerate the deployment of novel concepts, enabling scalable, sustainable and data-challenge-ready systems that redefine computing and sensing paradigms.

- **The Co-design and Heterogeneous Integration in Microelectronics for Extreme Environments (CHIME) Center**

CHIME aims to drive transformative advancements in extreme environment electronics through heterogeneous integration and a seamless fusion of diverse materials, processes and technologies to enable next-generation systems. The center will create robust, high-performance solutions capable of excelling in the most challenging conditions, including extreme thermal and radiation environments. Through co-design spanning materials, devices, circuits and systems, the center will harness interdisciplinary expertise to optimize technologies from the atomic scale to fully integrated instrumentation. The center's efforts will advance rapid prototyping methodologies to accelerate the innovation cycle, enabling swift iteration and validation of novel concepts. By bridging the gap from lab-to-fab, the center aims to translate research into scalable, manufacturable solutions that address critical societal and industrial needs.

- **The Extreme Lithography & Materials Innovation Center (ELMIC)**

ELMIC aims to advance the fundamental science driving the integration of new materials and processes into future microelectronic systems, focusing on key areas such as plasma-based nanofabrication, extreme ultraviolet (EUV) photon sources, 2D-material systems, and extreme-scale memory. The center's scientific investigations will be informed by a systems-to-physics motivation aimed at long-term impact.

The centers are formed as networks of 16 projects led out of 10 national laboratories. These projects were selected by competitive peer review under the DOE Laboratory Announcement 'Microelectronics Science Research Center Projects for Energy Efficiency and Extreme Environments."

Total funding is $179m for projects lasting up to four years in duration, with $41m in fiscal year 2024 and outyear funding contingent on congressional appropriations. The list of projects and more information can be found on the Office of Science program page.

Selection for award negotiations is not a commitment by DOE to issue an award or provide funding. Before funding is issued, DOE and the applicants will undergo a negotiation process, and the DOE may cancel negotiations and rescind the selection for any reason during that time.

https://science.osti.gov/

Sivers signs CHIPS Act contracts with Northeast Microelectronics Coalition Hub

First half of $11.6m Microelectronics Commons funding for 5G/6G and electronic warfare chip technology to be received in January

Sivers Semiconductors AB of Kista, Sweden (which supplies RF beam-former ICs for SATCOMs and photonic lasers for AI data centers) has signed contracts for both the electronic warfare and 5G/6G chip development awards with the Northeast Microelectronics Coalition (NEMC) Hub through the US CHIPS and Science Act. Funding is provided under the Microelectronics Commons program, executed through the Naval Surface Warfare Center (NSWC) Crane Division and the National Security Technology Accelerator (NSTXL).

Established in 2023 as one of eight regional Microelectronics Commons Hubs working to expand the USA's leadership in microelectronics and accelerate domestic semiconductor prototyping, the NEMC Hub is a division of the Massachusetts Technology Collaborative comprising a network of 200+ organizations including commercial and defense companies, leading academic institutions, federally funded R&D centers (FFRDCs), and startups concentrated in eight Northeast US states.

Sivers reckons that the awards further validate its wireless innovation as a critical enabler for mmWave technology adoption across markets. In these projects, Sivers will work with industry giants like BAE Systems, Raytheon and Ericsson and lead the commercialization of RF and beam-forming technology for defense and dual-use applications.

Advance payment of about half of the first-year value of both programs is expected to occur in January. If renewed over three years, under the discretion of future awards under the Microelectronics Commons program, the overall funding of both programs is expected to amount to about $30m.

"We are honored and grateful for these first two US CHIPS and Science Act funding awards and appreciate the support from the NEMC hub in helping find the right balance on associated contract structure and milestones," says Sivers Semiconductors' CEO Vickram Vathulya. "As we move forward with these critical portfolio projects, we remain committed to optimizing cash flow across all our development contracts, ensuring efficient working capital management while scaling our engagements."

"We're proud to collaborate with our partners on advancing RF technology for 5G/6G FR3 and electronic warfare," says Harish Krishnaswamy, managing director of Sivers Semiconductors' Wireless Division. "FR3 represents the next leap in cellular innovation, merging the superior range of sub-6GHz with the high-speed capabilities of millimeter-waves. Additionally, we're excited to broaden our portfolio with cutting-edge solutions for defense and electronic warfare, establishing a strong third pillar for our Wireless Division alongside SATCOM and 5G," he adds.

"Sivers Semiconductors is a key partner as we work to expand microelectronics lab-to-fab capabilities across the Northeast," comments NEMC Hub director Mark Halfman. "We are excited to collaborate on the development of critical technologies with opportunities for sustainable, positive impacts on our national security."

www.sivers-semiconductors.com
https://nemicroelectronics.org

Qorvo receives GSA award for Most Respected Public Semiconductor Company

Firm honoured for second time, for "leadership in diverse markets"

The Global Semiconductor Alliance (GSA) has named Qorvo Inc of Greensboro, NC, USA (which provides core technologies and RF solutions for mobile, infrastructure and defense applications) as the Most Respected Public Semiconductor Company in its category for 2024. Qorvo received the same award for the first time in 2022.

At its annual Awards Dinner, the GSA recognizes semiconductor companies that demonstrate excellence through their success, vision, strategy and future opportunities in the industry.

"Qorvo exemplifies leadership in diverse markets, combining advanced technologies and world-class design to tackle complex challenges," comments GSA president & co-founder Jodi Shelton. "Their innovation and strategy have cemented their role as a driving force in the semiconductor industry," she adds.

"For more than 40 years, our technology has been at the core of systems that connect, protect and power the planet," says Qorvo's president & CEO Bob Bruggeworth. "As we prepare to celebrate our tenth anniversary as Qorvo, this award reaffirms our ongoing commitment to delivering innovative solutions and building strong partnerships that drive progress."

www.gsaglobal.org/2024awd
www.qorvo.com

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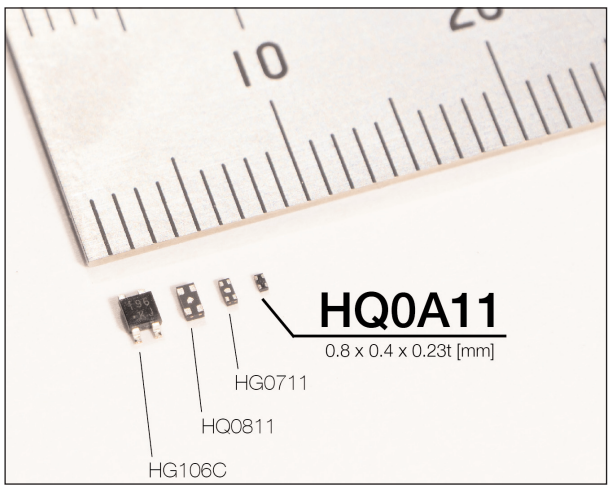
AKM ships its smallest and thinnest InAs Hall element, with volume shrunk by 85%

Position detection accuracy boosted 3.5-fold over GaAs Hall element

Japan-based Asahi Kasei Microdevices (AKM, a member of the Asahi Kasei Group's Material sector) has begun mass production and shipment of its next-generation indium arsenide (InAs) compound Hall element, which are used to detect magnetic fields (magnetic flux density).

Launched in November, the HQ0A11 features AKM's smallest and thinnest package size for an InAs-based Hall element, measuring 0.8mm x 0.4mm x 0.23mm. It achieves an 85% reduction in volume compared with the prior model HQ0811 in the high-sensitivity HQ series. The HQ0A11 is expected to contribute to improved performance in smartphone camera modules, small robots and other applications.

Smaller and thinner than the 1.6mm x 0.8mm x 0.38mm HQ0811 (previously the smallest and thinnest high-sensitivity Hall element), the HQ0A11 is also has an approximately 16% better signal-to-noise (S/N) ratio (which directly correlates to position detection accuracy) than HQ0811 (which previously had the highest S/N performance in the HQ series).



AKM started its Hall element business in 1974 with the development of sensors for automobile airbags. While advancing its development and manufacturing expertise to meet evolving market needs, AKM has shipped over 50 billion Hall sensors to date, including both Hall elements and Hall ICs.

Hall elements are often used for the position detection that is needed for image stabilization and autofocus in smartphone cameras. The demand for enhanced functionality and higher-resolution capture in cameras requires an increased component count within the same (or smaller) form factor, creating a growing need for ultra-compact products that enable high-density component mounting in a limited space.

The HQ0A11 is claimed to achieve the highest S/N performance among AKM products for position detection by leveraging the characteristics of InAs. Its position detection accuracy is over 3.5 times higher than that of the HG0C11, a gallium arsenide (GaAs) Hall element, which has been a mainstay product for camera modules. The HQ0A11 can hence significantly reduce the lens-shake effect that often occurs with smartphone cameras, especially with telephoto lenses.

AKM says that it will continue to leverage its proprietary compound semiconductor and packaging technology in order to further contribute to the miniaturization and improvement in performance of electronic products such as smartphones, small motors for robots, and other applications.

www.asahi-kasei.com/sustainability
www.akm.com

USPTO issues Notice of Allowance for AmpliTech's MMIC LNA patent application

Patent certificates expected to be issued during Q1–Q2/2025

AmpliTech Group Inc of Hauppauge, NY, USA — which designs, develops and makes signal-processing radio frequency (RF) microwave components and network solutions for satellite communications, telecoms (5G & IoT), space exploration, defense and quantum computing applications — says that the United States Patent and Trademark Office (USPTO) has issued another Notice of Allowance for its patent application related to its monolithic microwave integrated circuit (MMIC) low-noise amplifier (LNA) designs, based on its proprietary low-noise technology. The firm expects this and other previously announced patent certificates to be issued during Q1 and Q2/2025.

Upon issuance of this latest patent, AmpliTech says that it will hold three pivotal patents that encompass cutting-edge advances: cryogenic amplifiers tailored for the quantum computing market, optimized front-end modules for 5G radio networks, and MMIC designs leveraging proprietary LNA technology for diverse applications.

AmpliTech says that the pending new patent reflects its commitment to advancing its product offerings, expanding its intellectual property portfolio, and delivering high-performance solutions that empower customers to thrive in dynamic, future-forward markets.

www.amplitechgroup.com

Guerrilla RF unveils new GaN-on-SiC HEMT power amplifiers dice for high-performance RF

First in series provides up to 50W for custom MMICs

Guerrilla RF Inc (GRF) of Greensboro, NC, USA — which develops and manufactures radio-frequency integrated circuits (RFICs) and monolithic microwave integrated circuits (MMICs) for wireless applications — has formally released the GRF0020D and GRF0030D, the first in a new class of GaN-on-SiC HEMT power amplifiers being developed by the company. The unmatched discrete transistors provide up to 50W of saturated power for customers in the wireless infrastructure, military, aerospace and industrial heating markets looking to integrate bare die into their own custom MMICs.

Each device offers what is claimed to be exceptional flexibility, supporting either 50V or 28V supply rails while spanning multiple octaves of operational bandwidth for continuous wave, linear and pulsed modulation schemes. When using a 50V rail, the GRF0030D is rated for 50W (P_{SAT}) operation from DC to 6GHz, with gain varying from 13.5dB to 23.7dB. The device also supports 28V operation while delivering up to 27.5W of saturated output power. Similarly, the GRF0020D variant provides up to 30W and 19W of saturated power when using 50V and 28V rails, respectively. This slightly lower-power HEMT supports frequencies up to 7GHz while providing 13.8dB to 24.3dB of gain. As with all of Guerrilla RF's bare die offerings, each device is 100% DC production tested to ensure KGD (known good die) compliance.

According to market research from Yole Group, the RF GaN device market is growing from $1.3bn in 2022 to $2.7bn by 2028. This growth is driven by expansion in key segments relevant to Guerrilla RF, including telecom infrastructure (5G and point-to-point systems), military and satellite communications, with projected compound annual growth rates of 10%, 13% and 18%, respectively. Additionally, GaN-on-SiC variants are expected to dominate the market for the next decade.

"GaN technology is critical for next-generation, high-performance, energy-efficient RF systems and devices. We're already seeing strong demand for the GRF0020D and GRF0030D," notes CEO & founder Ryan Pratt. "Another advantage is that these devices are fabricated in the US, aligning with the objectives of the CHIPS Act of 2022 and ensuring a robust, domestic supply chain for our customers."

The GRF0020D and GRF0030D are available now for ordering, with samples ready for distribution. Pricing starts at $30 for 100-piece quantities. The bare dice are shipped in 2x2-inch waffle trays for safe transport and storage.

www.guerrilla-rf.com

Wolfspeed completes $200m at-the-market equity offering

Step to finalizing preliminary memorandum of terms for CHIPS funding

Wolfspeed Inc of Durham, NC, USA — which makes silicon carbide (SiC) materials and power semiconductor devices — has completed the offering of shares of its common stock under its previously announced 'at the market' (ATM) offering program pursuant to a shelf registration statement filed with the US Securities and Exchange Commission and a prospectus supplement dated 9 December.

Wolfspeed sold 27,793,535 shares for gross proceeds of about $200m. The firm will use the net proceeds to improve its capital structure, reduce leverage, and address outstanding maturities on its balance sheet.

"When I became executive chairman of Wolfspeed, completing our CHIPS Act funding process was a top priority of mine and today's news marks an important milestone in that regard," says executive chairman Tom Werner.

"With the ATM Program completed, we are now one step closer to finalizing our PMT [preliminary memorandum of terms] and receiving our first funding disbursements from the CHIPS office and our other lenders," he adds. "We look forward to continued collaboration with the CHIPS office to make sure the transition from silicon to silicon carbide is driven by American innovation, with American IP at the forefront."

www.wolfspeed.com

Wolfspeed launches Gen 4 MOSFET technology platform

Wolfspeed has introduced its new Gen 4 technology platform, which is said to enable design rooted in durability and efficiency, while reducing system cost and development time. Engineered to simplify switching behaviors and design challenges commonly experienced in high-power designs, Gen 4 charts a long-term roadmap across Wolfspeed's product categories, including power modules, discrete components, and bare die products. These products are currently available in the 750V, 1200V and 2300V classes.

"Each application's design comes with a unique set of requirements," notes Jay Cameron, senior VP of Wolfspeed power products. "From its inception, our goal for Gen 4 has been to improve overall system efficiency in real-world operating environments, with a focus on delivering maximum performance at the system level," he adds. "Gen 4 enables design engineers to create more efficient, longer-lasting systems that perform well in tough operating environments at a better overall system cost."

Silicon carbide technology is one of the fastest growing components of both the power device market and the greater semiconductor industry. A superior alternative to silicon, it is ideal for high-power applications — such as electric vehicle (EV) powertrains, e-mobility, renewable energy systems, battery energy storage systems, and AI data centers — that unlocks improved performance and lower system costs.

Wolfspeed says that, as the USA and the globe pursue more efficient and environmentally friendly solutions to meet the ever-increasing need for high-voltage energy sources, it is crucial that the USA continues to make strategic investments, while continuing to spur American innovation in critical technologies.

Wolfspeed is the only silicon carbide producer with both silicon carbide material and silicon carbide device fabrication facilities based in the USA, a factor that is becoming increasingly important under the new US Administration's increased focus on national security and investment in US semiconductor production.

"Innovative technology unlocks business opportunity," says Devin Dilley, president & chief product officer at US-based utility-scale inverter manufacturer EPC Power. "Wolfspeed's new Gen 4 SiC technology is enabling EPC Power to make a paradigm shift in how energy is created and stored globally," he adds.

"Our Gen 4 platform will be delivered via our highly efficient 200mm wafers, which will enable us to deliver products on a scale and level of yield not seen in this industry before," says Wolfspeed's executive chairman Tom Werner.

Wolfspeed's Gen 4 platform was designed to comprehensively improve system efficiency and prolong application life, even in the harshest of environments, while helping to reduce system cost and development time. The technology should deliver significant performance enhancements for designers of high-power automotive, industrial and renewable energy systems, with key benefits including:

- **Holistic system efficiency**: Delivering up to a 21% reduction in on-resistance at operating temperatures with up to 15% lower switching losses.
- **Durability**: Ensuring reliable performance, including a short-circuit withstand time of up to 2.3µS to provide additional safety margin.
- **Lower system cost**: Streamlining design processes to reduce system costs and development time.

Wolfspeed's Gen 4 products are available in 750V, 1200V and 2300V nodes, with options for power modules, discrete components, and bare die products. New product introductions, including additional footprints and R_{DSON} ranges, will be available throughout 2025 and early 2026.

Indichip to construct $1.4bn silicon carbide fab

India's first private semiconductor manufacturing facility to be dedicated to SiC

India's Indichip Semiconductors Ltd has signed a memorandum of understanding (MoU) with the government of Andhra Pradesh state to construct 'India's first private semiconductor manufacturing facility'.

Dedicated to manufacturing silicon carbide (SiC) power devices, the commitment aligns with the Indian government's 'self-reliant India' ('Atma-nirbhar Bharat') initiative, which aims to reduce dependency on imports and foster local capabilities. By driving local innovation and production, Indichip aims to deliver advanced technology that not only meets international standards but also addresses local needs.

The local production of SiC devices also fills a gap in India's semiconductor supply chain, allowing the country to boost its self-sufficiency in a sector facing high demand. Currently, India imports over 90% of its semiconductor components.

TG Bharath, Industries Minister for the Andhra Pradesh administration confirmed in a posting on X that the memorandum of understanding was worth Rs14,000 crore (US$1.4bn) and that the site would be located in Kurnool district at the Orvakal Mega Industrial Hub, which is part of the Hyderabad Bengaluru Industrial Corridor (HBIC).

The agreement was brokered by the government of Andhra Pradesh, along with representatives of Indichip and its Japanese strategic technology transfer partner Yitoa Micro Technology Corp (YMTL). Andhra Pradesh launched a semiconductor policy in November 2024 to promote the state as a hub for electronics and semiconductor manufacturing.

The MoU was signed between Indichip's managing director Piyush Bichhoriya and Andhra Pradesh Economic Development Board's CEO Saikanth Varma in the presence of Nara Lokesh (the minister for information technology, electronics and HRD), TG Bharath (minister for industries), and representatives from Indichip and YMTL.

The fabrication plant will launch with an initial production capacity of 10,000 wafers per month, rising to 50,000 wafers per month within 2–3 years.

Indichip's initial efforts will be on 6-inch SiC wafers, with plans to transition to 8-inch wafers in the future, not only enhancing performance but also aligning with global production standards.

www.indichipsemiconductors.com/post/unveiling-indichip-

SemiQ launches QSiC 1700V series of high-reliability, low-loss SiC MOSFETs targeting renewables, energy storage and EV charging applications

AEC-Q101-qualified bare die and discrete packaged devices WLBI screened and tested to avalanche breakdown over 2200V; power and half-bridge modules available to simplify system design

SemiQ Inc of Lake Forest, CA, USA — which designs, develops and manufactures silicon carbide (SiC) power semiconductors and 150mm SiC epitaxial wafers for high-voltage applications — has announced a family of 1700V SiC MOSFETs designed to meet the needs of medium-voltage high-power conversion applications, such as photovoltaic and wind inverters, energy storage, electric vehicle (EV) and road-side charging, uninterruptable power supplies, and induction heating/welding.

The high-speed QSiC 1700V switching planar D-MOSFETs enable more compact system designs at large scale, with higher power densities and lower system costs. They feature a reliable body diode, capable of operation at up to 175ºC, with all components tested to beyond 1900V, and UIL avalanche tested to 600mJ.

The QSiC 1700V devices are available both in a bare die form (GP2T030A170X) and as a 4-pin TO-247-4L-packaged discrete (GP2T030A170H) with drain, source, driver source and gate pins. Both are also available in an AEC-Q101 automotive-qualified version (AS2T030A170X and AS2T030A170H).

The MOSFETs deliver low switching and conduction losses, low capacitance and feature a rugged gate oxide for long-term reliability, with 100% of components undergoing wafer-level burn in (WLBI) to screen out potentially weak oxide devices.

SemiQ has also announced a series of three modules as part of the family to simplify system design, including a standard-footprint 62mm half-bridge module housed in an S3 package with an AlN insulated baseplate, as well as two SOT-227 packaged power modules.

Specifications

The QSiC 1700V series' bare die MOSFET comes with an aluminium (Al) top side and nickel/silver (Ni/Ag) bottom side. Both it and the TO-247-4L packaged device have a power dissipation of 564W, with a continuous drain current of 83A (at 25ºC, 61A at 100ºC) and a pulsed drain current of 250A (at 25ºC). They also feature a gate threshold voltage of 2.7V (at 25ºC, 2.1V at 125ºC), an R_{DSON} of 31mΩ (at 25ºC, 57mΩ at 125ºC), a low (10nA) gate–source leakage current and a fast reverse recovery time (t_{RR}) of 17ns.

The TO-247-4L package has a junction-to-case thermal resistance of 0.27ºC per watt.

The two 4-pin power modules have a 38.0mm x 24.8mm x11.7mm SOT-227 design and deliver an increased power dissipation of 652W with an increased continuous drain current of 123A (at 25ºC — GCMX015A170S1E1) and 88A (at 25ºC GCMX030A170S1-E1). In addition to low switching losses, both modules have a low junction-to-case thermal resistance of 0.19ºC and 0.36ºC per watt and feature an easy-mount design for direct mounting of the isolated package to a heatsink.

The half-bridge module is housed in a 61.4mm x106.4mm x 30.9mm 9-pin S3 package and delivers a power dissipation of 2113W with a continuous drain current of 397A and a pulsed drain current of 700A. In addition to low switching losses, the GCMX005A170S3B1-N module has a junction-to-case thermal resistance of 0.06ºC per watt.

www.semiq.com/module-packages
www.semiq.com/mosfets-packages

onsemi completes acquisition of Qorvo's silicon carbide JFET business for $115m

United Silicon Carbide subsidiary expands market opportunity by $1.3bn by 2030

Intelligent power and sensing technology firm onsemi of Scottsdale, AZ, USA has completed its acquisition of the silicon carbide junction field-effect transistor (SiC JFET) technology business, including the United Silicon Carbide subsidiary, of Qorvo Inc of Greensboro, NC, USA (which provides core technologies and RF solutions for mobile, infrastructure and defense applications) for $115m in cash.

onsemi says that the addition of SiC JFET technology will complement its EliteSiC power portfolio and enable it to address the need for high energy efficiency and power density in the AC–DC stage in power supply units for artificial intelligence (AI) data centers. In electric vehicle applications, SiC JFETs help to improve efficiency and safety by replacing multiple components with a solid-state switch based on SiC JFET in battery disconnect units. In the industrial end-market, SiC JFETs enable certain energy storage topologies and solid-state circuit breakers.

"This acquisition further strengthens onsemi's leadership in power semiconductors by providing disruptive and market-leading technologies to our customers to solve their most pressing power density and efficiency problems in AI data centers, automotive and industrial markets," reckons Simon Keeton, group president & general manager of onsemi's Power Solutions Group. "We will continue to innovate and make investments to expand our technology leadership in providing the most comprehensive power system solutions."

onsemi reckons that, by strengthens its position in high- and mid-voltage power semiconductors, the acquisition will expand its market opportunity by $1.3bn by 2030.

www.onsemi.com

MACOM unveils five-year, $345m plan to expand 100mm GaN and GaAs production and introduce 150mm GaN

Up to $180m of CHIPS Act investment for Massachusetts and North Carolina fabs

MACOM Technology Solutions Inc of Lowell, MA, USA (which designs and makes RF, microwave, analog and mixed-signal and optical semiconductor technologies) has announced a long-term capital investment plan comprising up to $345m over five years to modernize its wafer fabrication facilities in Lowell, Massachusetts, and Durham, North Carolina, creating up to 350 manufacturing jobs and nearly 60 construction jobs across both states.

The plan is supported by a recently executed preliminary, non-binding agreement with the CHIPS Program Office, which would provide for proposed direct funding from the US Department of Commerce under the CHIPS and Science Act of up to $70m.

The preliminary terms propose up to $180m to be supported by the CHIPS and Science Act through a combination of direct federal funding, federal investment tax credits and state funding, including direct funding from the Massachusetts Technology Collaborative (MassTech) of up to $15.7m as well as other incentives from the State of Massachusetts.

The balance of about $165m is expected to be self-funded by MACOM's operating cash flow over the next five years.

MACOM says that the wafer fab capital investment plan supports its growth and market positioning strategy to be an industry-leading supplier of advanced RF, microwave and millimeter-wave semiconductor technologies, supporting existing and emerging defense, telecoms and data-center applications.

Both fabs are Category 1A Trusted Foundries with the US Department of Defense (DoD) and produce compound semiconductors that are key to defense systems operating at high frequencies, including airborne and ground-based radar systems, as well as commercial applications such as telecoms.

Massachusetts fab investment

- expansion of cleanrooms within existing building footprint;
- modernization of existing 100mm production lines, including gallium arsenide (GaAs), gallium nitride (GaN), silicon and other III-V materials;
- installation of 150mm GaN-on-SiC manufacturing capability for advanced-node applications;
- infrastructure upgrades (HVAC, water, solar and power systems).

North Carolina fab investment

- expansion of cleanrooms within existing building footprint;
- installation of 150mm wafer-size production capabilities to support RF GaN-on-SiC processes;
- installation of advanced metal-organic chemical vapor deposition (MOCVD) epitaxial growth capabilities;
- infrastructure upgrades (HVAC, water, power systems).

"This plan will strengthen MACOM's domestic semiconductor manufacturing capabilities, accelerate our growth strategy and enable us to better service our customers with leading technologies," says president & CEO Stephen G. Daly.

MACOM expects to work with the CHIPS Program Office to finalize the details and terms of a definitive agreement.

www.chips.gov
www.macom.com
www.masstech.org

MACOM signs preliminary memorandum of terms for US CHIPS Act funding

Lowell project to be supported by $15.7m in state match funding

MACOM Technology Solutions Inc of Lowell, MA, USA (which designs and makes RF, microwave, analog and mixed-signal and optical semiconductor technologies for the commercial and defense sectors) has signed a preliminary memorandum of terms with the US federal government for funding under the CHIPS for America program.

Announced on 14 January by the US Department of Commerce, the proposed funding will include support for a project to expand and modernize MACOM's Lowell manufacturing facility and semiconductor wafer foundry with new cleanrooms, equipment, wafer fabrication stations, chip-level packaging, and test capacity. The new project is estimated to add up to 150 new jobs, two-thirds of which are expected to be skilled positions. The expansion will require the addition of technicians, engineers, program managers, sales and maintenance positions that will be filled through partnerships with local educational institutions, including UMass Lowell and UMass Amherst.

In addition to the announced federal funding terms, the $172m project will be supported by an expected $15.7m from the Massachusetts Technology Collaborative (MassTech) as well as other federal tax incentives and private investment from MACOM. These incentives are contingent upon MACOM finalizing their federal funding award.

This is the second major microelectronics announcement in Lowell in the past year following the launch in March 2024 of the new Lowell Innovation Network Corridor (LINC) project, a public–private partnership that aims to bring technology jobs and housing to the city. The project will include the establishment of a new research building on UMass Lowell's East Campus that will house the microelectronics division of Cambridge's Draper Laboratory.

"Through MACOM's expansion, coupled with the LINC project, we have the opportunity to transform Lowell and the Merrimack Valley into a powerhouse for microelectronics and semiconductor development," believes Massachusetts Economic Development Secretary Yvonne Hao. "By adding critical domestic production and increasing our talent pool of highly qualified workers we will advance our standing in the CHIPS community," she adds.

In May 2023, MassTech launched an online portal that created a 'digital front door' for Massachusetts companies to request state support, a key requirement of the grant programs established under the CHIPS and Science Act. The portal was constructed in partnership with the Executive Office of Economic Development, the Massachusetts Office of Business Development (MOBD) and other state agencies that helped to streamline the process to engage with state funding options.

Innovative companies like MACOM are strategically focused on expanding microelectronics capacities in both commercial and defense applications," notes Massachusetts Technology Collaborative chief investment strategist Ben Linville-Engler. "Their pursuits of CHIPS funding are being strengthened by the state's federal matching commitment."

"Innovative companies like MACOM are strategically focused on expanding microelectronics capacities in both commercial and defense applications," notes Massachusetts Technology Collaborative deputy director & chief investment strategist Ben Linville-Engler. "Their pursuits of CHIPS funding are being strengthened by the state's federal matching commitment."

The Massachusetts-based incentives are part of the state's efforts to bolster state-based organizations pursuing US CHIPS and Science Act funding. In addition to support for individual submissions to the US Department of Commerce's incentive program, the state is also managing CHIPS-related investments through the work of the Northeast Microelectronics Coalition (NEMC) Hub, a division of MassTech that is leading a regional collaboration of more than 200 organizations, including MACOM. The Northeast has been the recipient of a number of other CHIPS-funded awards, including:

- A $37.8m Microelectronics Commons award to the NEMC Hub to advance the development of microelectronics technologies in the Northeast.
- The launch of NEMC Hub' $2.5m Powering Regional Opportunities for Prototyping Microelectronics (PROPEL) program to help startups and small businesses to defray development costs, helping to accelerate the lab-to-fab transition of innovative microelectronics technologies.
- $1.5m to boost four workforce development, education and student engagement programs across the Northeast.
- A $7.7m award to establish new 'open access' advanced nanofabrication capability within the MIT.Nano research hub in Cambridge, a collaborative project with Applied Materials.

www.chips.gov
www.masstech.org
www.macom.com
www.draper.com

Vermont Gallium Nitride Tech Hub awarded $23.7m from US Economic Development Administration

Twelve companies already committed to accelerating product development through V-GaN Tech Hub

The Vermont Gallium Nitride (V-GaN) Tech Hub — a consortium led by the University of Vermont (UVM) and including GlobalFoundries and the State of Vermont — has been awarded $23.7m in federal funding from the US Economic Development Administration (EDA).

The Vermont Tech Hub will create a technology ecosystem in the Green Mountain State and New England to drive design and manufacturing of high-power and high-frequency GaN semiconductors. Pairing GlobalFoundries' semiconductor expertise with UVM's researchers, the Tech Hub aims to fuel business growth and workforce development to enhance the region's and state's economic and social vitality — bringing new facilities and computing technology to Vermont.

The Tech Hub will train over 500 new staff in the semiconductor workspace and engage over 6000 K-12 students across Vermont in STEM participation in the next five years.

The federal funding "solidifies UVM's position as a national leader in research and workforce development within this critical technological field," reckons UVM interim president Patricia Prelock.

Vermont's Tech Hub is one of six federal hubs awarded a total of $210m in funding in this cycle. The investment is intended to advance innovative projects in Vermont promoting GaN technology, economic growth, and workforce development, including:

- **Advanced Design Computing Center**:
A facility offering start-ups affordable access to advanced GaN and semiconductor design tools, reducing financial risks and fostering innovation. Partnering with UVM's Vermont Advanced Computing Center, it will support commercial and national security applications, driving next-gen computing solutions.
- **Test and Characterization Lab (TCL)**:
Located at OnLogic in South Burlington, V-GaN's TCL will be the only publicly accessible lab in the USA offering comprehensive testing and technical advice for high-power and high-frequency GaN devices. Its capabilities were developed with input from key stakeholders, including GlobalFoundries, UVM's College of Engineering and Mathematical Sciences, and smaller regional semiconductor firms.
- **V-GaN Training, Innovation, Design and Engineering (TIDES)**:
UVM's Professional and Continuing Education division will lead this major workforce development effort, offering K-12 initiatives to spark interest in GaN technologies, career pathways to increase rural access to semiconductor manufacturing jobs, and continuing education in semiconductor design, manufacturing, and GaN-specific skills. Partners include the Community College of Vermont, Norwich University, the Vermont State University System, and the Vermont Manufacturing Extension Center.

Electrical engineering students use UVM semiconductor technology with GlobalFoundries staff.

"Global demand for GaN and related semiconductor solutions is rapidly increasing, and we are determined to meet that demand," says Kirk Dombrowski, UVM's vice president for Research and Economic Development. "GaN not only holds promise for a wide range of applications in the technology space, it also provides an opportunity for V-GaN Tech Hub members to make northern New England the global leader in that space," he adds. "This work benefited from the participation of more than 30 UVM partners — including GlobalFoundries, OnLogic, Cadence, and the Vermont Center for Emerging Technologies — and represents the next generation of UVM's land grant mission."

Twelve companies have already committed to accelerating their product development through the V-GaN Tech Hub. It will make grant funding available to offset development costs for businesses owned by under-served and under-represented populations in the semiconductor industry.

www.uvm.edu
www.vgan.tech

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or contact us: x-fea-fuji-dc@fujielectric.com

Odyssey announces liquidation distribution

Odyssey Semiconductor Technologies Inc of Ithaca, NY, USA says that its only, and final, liquidating distribution is $0.11 per share, paid on or about 23 December, to holders of its common stock, as of the record date of 19 August.

Odyssey was a developer of high-voltage vertical power switching components based on proprietary gallium nitride (GaN) processing technology. But on 7 May, it was announced that its assets were to be acquired by Power Integrations Inc of San Jose, CA, USA (which provides high-voltage integrated circuits for energy-efficient power conversion), with all key Odyssey employees joining Power Integrations' technology organization. The acquisition was completed on 1 July.

Pursuant to Odyssey's plan of complete liquidation, dissolution and distribution of assets, approved by the stockholders special meeting on 3 June, the distribution will result in the complete redemption and cancellation of all of the outstanding capital stock.

As of 17 December, Odyssey has a cash balance of about $1.837m. At the board of directors' discretion, after payment of $0.11 per share, or $1,606,096.91 in total for the distribution, the company has reserved cash of about $61,000 for payments for federal and state tax liabilities and related expenses, and $169,000 for legal and other third-party dissolution expenses and both accrued and anticipated obligations.

Following the distribution, the company will file a verified petition with the Delaware Court of Chancery to seek a court order to determine the amount of cash reserves, if any, to be set aside as a securiey to address any potential claims, if any, that may arise against it.

www.odysseysemi.com
www.power.com

Power Integrations adds wide-creepage switcher IC for 800V automotive applications

1700V InnoSwitch3-AQ flyback switcher for IEC60664-1 isolation standard

Power Integrations Inc of San Jose, CA, USA (which provides high-voltage integrated circuits for energy-efficient power conversion) has introduced a wide-creepage package option for its InnoSwitch3-AQ flyback switcher IC for automotive applications. A wide drain-to-source-pin creepage distance of 5.1mm eliminates the need for conformal coating, making the IC compliant to the IEC60664-1 standard in 800V electric vehicles (EVs) while simplifying manufacturing and increasing system reliability.

"Automotive designers rely on the efficiency and low component count of high-voltage power supplies designed around InnoSwitch3-AQ ICs," notes Power Integrations' product marketing engineer Mike Stroka. "The increased primary-to-primary creepage and clearance distance between the drain and source pins in the new package provides support for the next generation of EV bus voltages," he adds. "Power Integrations' unique InSOP-28G package enables 1000V_{DC} to be provided to the primary side, while keeping all other pins safely isolated in pollution degree 2 environments."

The 1700 V-rated CV/CC InnoSwitch3-AQ switching power supply ICs incorporate a silicon carbide (SiC) primary switch capable of delivering up to 80W of output power. The highly integrated ICs reduce the number of components required to implement a power supply by as much as 50%, saving space, enhancing system reliability and mitigating component sourcing challenges. An increased drain-pin width is beneficial in withstanding high levels of shock and vibration, especially in eAxle automotive applications.

The new members of the InnoSwitch3-AQ family will start up with as little as 30V on the drain without external circuitry, which is critical for functional safety. Additional protection features include input under-voltage, output over-voltage and over-current limiting. Synchronous rectification and a multi-mode valley switching, discontinuous/continuous conduction mode (DCM/CCM) flyback controller deliver over 90% efficiency. Devices consume less than 15mW at no-load.

Target automotive applications include battery management systems, µDC–DC converters, control circuits and emergency power supplies in the main traction inverter. The ICs also have improved functionality for remote on/off.

Pricing for the new 1700V-rated InnoSwitch3-AQ switching power supply ICs starts at $6 per unit for 10,000-unit quantities.

Sample ICs are available now, with full production in first-quarter 2025, via sales representative or authorized worldwide distributors DigiKey, Newark, Mouser and RS Components.

www.power.com

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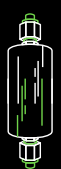
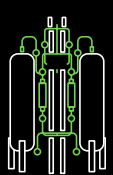
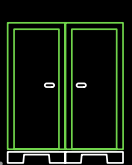


Point-of-Use Purifiers



Frame-Mounted Purifiers



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InnoScience floats in IPO on Hong Kong Stock Exchange

ST Hong Hong takes a quarter of offer shares

Shares in China-based gallium nitride-on-silicon (GaN-on-Si) power chip maker InnoScience (Suzhou) Technology Holding Co Ltd began trading on 30 December after being listed on the Main Board of the Hong Kong Stock Exchange in an initial public offering (IPO) of 45.36 million shares at HK$30.86 each, raising gross proceeds of HK$1.4bn (US$180m). The offer price range had been HKD30.86–33.66, aiming to raising up to HKD1.527bn ($193m).

The total number of issued shares is 879.155 million, giving InnoScience total market value of HK$27bn.

Of the offer shares, 55.38% were taken up by four cornerstone investors: ST Hong Hong (which is a subsidiary of Europe-based STMicroelectronics Ltd) at US$50m (comprising 27.76% of offer shares and 1.43% of share capital), Jiangsu Govtor Inno Technology Ltd (a subsidiary of the Jiangsu State-owned Enterprise Mixed Ownership Reform Fund) at US$25m (13.88% of offer shares, and 0.72% of share capital), and HK InnoSC Ltd (a subsidiary of the Jiangsu Suzhou High-end Equipment Industry Special Parent Fund) and Inno CL (a subsidiary of Suzhou Oriental Chuanglian Investment Management) each at US$12.5m (6.87% of offer shares, and 0.35% of share capital).

InnoScience aims to use 60% of the IPO's net proceeds of HK$1.3bn to expand capacity for its 8-inch GaN wafers over the next five years from 12,500 wafers per month in 2024 to 70,000wpm in 2029, and 20% for R&D and to expand the firm's product portfolio.

https://www.ipox.com/upcoming-ipos

Innoscience files lawsuits against Infineon in China

InnoScience (Suzhou) Technology Holding Co Ltd and its subsidiary InnoScience (Suzhou) Semiconductor Co Ltd have filed complaints regarding patent 202311774650.7 and 202211387983.X with the Intermediate People's Court of Suzhou City, Jiangsu Province, against Infineon Technologies (China) Co Ltd, its subsidiary Infineon Technologies (Wuxi) Co Ltd, and Suzhou Chipswork Electronics Technologies Co Ltd.

The patents relate to a gallium nitride (GaN) power device and preparation method, and a nitride-based semiconductor device and method for manufacturing it, respectively. According to the complaints, Infineon Technologies (Wuxi) Co Ltd is the filing entity of Infineon's Chinese website, which displays, advertises and sells various models of GaN devices to potential customers in China. Infineon Technologies (China) Co Ltd is importer and general distributor of the infringing products involved. According to Infineon's Chinese website, Suzhou Chipswork Electronics Technologies Co Ltd is the value-added distributor of Infineon Technologies (China) Co Ltd and Infineon Technologies (Wuxi) Co Ltd in China.

After technical comparison, InnoScience believes that the infringing products fall within the scope of protection of the patents involved. The three defendants, without InnoScience's permission, implemented the offer for sale, sale and import of the infringing products, constituting patent infringement, and should bear the corresponding legal responsibilities in accordance with the laws, including ceasing infringement and assuming liability for compensation, says InnoScience.

EPC Space achieves JANS MIL-PRF-19500 certification

EPC Space LLC of Haverhill, MA, USA (which provides high-reliability radiation-hardened enhancement-mode gallium nitride-on-silicon transistors and ICs for power management in space and other harsh environments) says that both its facility in Andover, Massachusetts, and its wafer fabrication facility in Taiwan have been certified under the JANS MIL-PRF-19500 standard.

EPC Space says that certification highlights its role in providing semiconductors for critical space applications. Managed by the US Department of Defense, the MIL-PRF-19500 certification sets the bar for reliability, performance and environmental resilience in semiconductor components. EPC Space claims that its achievement in obtaining this certification for GaN HEMT is a world first.

"Securing the JANS certification is a direct result of our relentless pursuit of quality," says EPC Space's CEO Bel Lazar. "Our teams have worked tirelessly to ensure our products not only meet but exceed the expectations for reliability in the most demanding conditions," he adds.

"The commitment to the MIL-PRF-19500 standard not only guarantees the durability and performance of EPC Space's products but also reinforces the company's dedication to supporting its customers in achieving their critical objectives," says Alex Lidow, CEO of EPC Corp.

Looking ahead, EPC Space is set to launch 18 JANS-certified rad-hard GaN HEMT parts, ranging from 40V to 300V, throughout 2025.

www.epc.space

Innoscience expands 100V automotive-grade portfolio

$R_{DS(on),max}$ = 13.5mΩ and smaller-package 80mΩ devices optimized for LiDAR plus high-power-density DC–DC converters and Class D audio

Gallium nitride-on-silicon (GaN-on-Si) power solutions firm Innoscience of Suzhou, China has expanded its portfolio with two 100V automotive-grade GaN devices.

The INN100W135A-Q ($R_{DS(on),max}$ = 13.5mΩ) and smaller-package INN100W800A-Q ($R_{DS(on),max}$ = 80mΩ) are both certified to AEC-Q101 and optimized for LiDAR as well as for high-power-density DC–DC converters, and Class D audio applications in the automotive sector.

The INN100W135A-Q and the ultra-compact INN100W800A-Q, with a WLCSP package measuring 2.13mm x 1.63mm and 0.9mm x 0.9mm respectively, are said to offer significant advantages in terms of size and power efficiency. Both devices are specifically tailored for the requirements of L2+/L3 assisted driving systems, with switching speeds up to 13 times faster and pulse widths reduced to one-fifth of those of silicon solutions. Parameters like Q_g and Q_{oss} are also improved by 1.5–3 times over their silicon counterparts. This results in medium- to long-range recognition capabilities of 200/300m, which is essential for advanced driver assistance and autonomous driving applications.

"Both devices have been designed to meet the growing demand for efficiency and precision in driving assistance and autonomous driving technologies — GaN devices are rapidly replacing traditional silicon in critical automotive applications due to their superior performance," notes Dr Denis Marcon, general manager, Innoscience Europe. "In LiDAR applications, it is well understood that GaN enables higher resolution and greater detection distances while reducing power loss and temperature rise than is possible with traditional silicon technology."

These automotive-grade GaN products have already entered mass production, with batch orders being fulfilled to meet demand.

www.innoscience.com

EPC introduces fully configured motor drive inverter reference design

Optimized PCB layout for wide input voltage range and versatility

Efficient Power Conversion Corp (EPC) of El Segundo, CA, USA — which makes enhancement-mode gallium nitride on silicon (eGaN) power field-effect transistors (FETs) and integrated circuits for power management applications — has introduced the EPC91200, a fully configured motor drive inverter reference design that is said to deliver exceptional performance and flexibility for a variety of industrial and battery-powered applications.

Optimized for wide voltage ranges and versatility

The EPC91200 is designed for 3-phase brushless DC (BLDC) motor drive applications and features the EPC2305, a 150V 3mΩ $R_{DS(on)}$ GaN FET. The EPC91200 supports wide voltage ranges from 30V to 130V, making it suitable for 80V and 110V battery systems commonly used in industrial automation, agricultural machinery, and material handling equipment such as forklifts.

Highlights include:

- High current capacity: supports up to 60Apk (40A_{RMS}) maximum output current with a switching frequency of up to 150kHz;
- Enhanced efficiency: optimized PCB layout and advanced GaN technology reduce resistance and heat generation for improved performance;
- Integrated features: includes current sensing, voltage monitoring, overcurrent protection, and temperature sensing for robust operation;
- Compatibility: Works with multiple controller boards from leading manufacturers such as STMicroelectronics, Texas Instruments, and Microchip.

Design benefits

The EPC91200 is said to streamline the development process with features tailored for quick deployment and evaluation. The compact design (130mm x 100mm) includes a pre-configured shaft encoder/Hall sensor interface and supports field-oriented control (FOC) techniques. Engineers can easily measure critical signals and optimize system performance using built-in test points.

"With the EPC91200, we provide engineers a versatile, off-the-shelf motor drive solution, showcasing the efficiency, reliability and adaptability of GaN technology in modern power systems," says CEO Alex Lidow.

The EPC91200 reference design boards are priced at $780. The EPC2305 is priced at $3.56/each in 3Ku reels. Reference design boards and devices are available for immediate delivery from distributor Digi-Key Corp.

www.epc-co.com/epc/products/evaluation-boards/epc91200

Aehr's quarterly revenue hit by order delays

Silicon carbide to comprise under half of full-year revenue as AI, gallium nitride and silicon photonics business grows

For its fiscal second-quarter 2025 (ended 29 November 2024), semiconductor production test and reliability qualification equipment supplier Aehr Test Systems of Fremont, CA, USA has reported revenue of $13.5m, up slightly from $13.1m last quarter but down on $21.4m a year ago. While Services revenue has rebounded from $0.97m last quarter to $1.47m, Product revenue has fallen further, from $19.8m a year ago and $12.2m last quarter to $12m.

"Given the nature of our business with our high ASPs, our quarterly revenue can experience significant variability if system orders anticipated by quarter-end are delayed by even a few days. This was the case in this last quarter," notes president & CEO Gayn Erickson.

Recent business highlights include securing:

- the first artificial intelligence (AI) processor customer for wafer-level burn-in, utilizing the new high-power FOX-XP solution for wafer-level production test & burn-in of AI processors.
- the first volume production orders from an AI processor customer for package-part burn-in, utilizing recently acquired Sonoma ultra-high-power systems for high-volume production test & burn-in of AI processors.
- the first gallium nitride (GaN) customer for high-volume production wafer-level burn-in of GaN devices using the FOX-XP platform.

"In the case of both our new GaN and wafer-level AI customers, both requested pre-built systems that we fully expected to ship to them within the quarter. However, the purchase orders were not finalized until after the quarter ended," says Erickson.

On a non-GAAP basis, operating expenses have risen further, from $4.95m a year ago and $5.52m last quarter to $5.89m.

Net income has fallen further, from $6.73m ($0.23 per diluted share) a year ago and $2.15m ($0.07 per diluted share) last quarter to just $0.69m ($0.02 per diluted share).

During the quarter, total cash, cash equivalents and restricted cash fell from $40.8m to $35.2m.

Order bookings were $9.2m, down from $16.8m last quarter but still well above the low of just $4m the quarter before that. Order backlog fell back during the quarter from $16.6m to $12.4m. However, effective backlog (including bookings taken since 29 November) is $26.6m.

Diversification of markets and customers

"We achieved significant progress on the key objectives we outlined at the start of the fiscal year, most notably expanding our product reach into additional large and fast-growing markets," notes Erickson. "Market diversification into AI processors, gallium nitride power semiconductors, data storage devices, silicon photonics integrated circuits, and flash memory is driving new opportunities in terms of customers and revenue. This progress includes our wafer-level burn-in solutions and also the success we're achieving with the new semiconductor package-part test & burn-in product line from the acquisition of Incal Technology we closed last August. The acquisition has led to the acceleration of our market diversification with particular success and leverage expanding our total available market (TAM) in AI processors," he adds.

"Last month, we reached a significant milestone by securing our first AI processor customer for wafer-level burn-in. This includes initial volume production orders for multiple high-power FOX-XP systems and our proprietary WaferPak Contactors, which enable full-wafer contact for testing & burn-in of AI processors in wafer form before system integration. This achievement represents a technological and commercial breakthrough for Aehr, significantly expanding the market potential for our FOX-XP wafer-level test & burn-in systems.

"During the quarter, we secured our first production AI processor customer for package-part burn-in, receiving initial volume production orders for multiple Sonoma ultra-high-power systems. This customer is a large-scale data-center hyperscaler and provides computing power and storage capacity to millions of individuals and organizations worldwide. System shipments have already commenced to their contract manufacturer doing test & burn-in for them in Asia. We see a significant potential to expand our packaged-part test & burn-in business with the product line acquired from Incal, and feel we are particularly well positioned to capitalize on opportunities in the rapidly growing AI semiconductor market with the ultra-high-power Sonoma product line. We estimate that the combined wafer-level and package-part reliability test and production burn-in market for AI processors will exceed $100m annually in the future and, with our comprehensive product portfolio, we believe we can capture a meaningful share of this market," says Erickson.

"Last week we announced another exciting milestone with our first gallium nitride (GaN) semiconductor production order. This achievement expands our production wafer-level burn-in market for power semiconductors beyond silicon carbide used in electric vehicles, data-center power conversion and solar to now include GaN, a high-performance compound semiconductor optimized for mid-power applications such as data centers, solar energy, automotive systems,

and consumer computing. Over the past 12 months, we have collaborated with this lead customer using our FOX-NP system, leading to their purchase of multiple WaferPak reference designs for diverse GaN applications. GaN offers a broader application range than silicon carbide and is poised for significant growth in the coming decade. With an expected compound annual growth rate (CAGR) exceeding 40%, the GaN market is projected to surpass $2bn in annual device sales by 2029, according to Yole Group's 'Power SiC/GaN Compound Semiconductor Market Monitor'. Additionally, Frost & Sullivan estimates that GaN semiconductors will account for over 10% of the worldwide power semiconductor industry by 2028. This transformative technology represents a significant growth opportunity for Aehr's wafer-level test & burn-in solutions, positioning us to capitalize on the rapid expansion of the GaN market," reckons Erickson.

"In addition, we are excited about our opportunity for production burn-in and stabilization of devices used in hard disk drives using our FOX-CP systems and WaferPak Contactors. Our lead customer for this application is ramping this year and has told us that they will purchase multiple production systems from us over the next few quarters to support their planned new product rollout and ramp. This customer, first announced back in 2019 prior to the COVID-19 pandemic, initially purchased our FOX-CP single-wafer test & burn-in solution to support the qualification and early test stages of this new product aimed at the enterprise and data-center markets. We view the data storage market both for hard disk drives and flashed-based semiconductor solid-state disk drives as significant growth opportunities for our systems. These markets have applications with devices made up of multiple die in complex structures, or in multiple die stacked on top of each other before they are put into higher-level packages or systems. These devices require exceptionally high levels of quality and long-term reliability of the die before they are put into these packages or systems, which aligns perfectly with the capabilities of our wafer-level test & burn-in systems," says Erickson.

"Aehr also continues to expand its presence in the silicon carbide power semiconductor market, a critical sector for power conversion for electric vehicle traction inverters, charging infrastructure, and a range of industrial, data-center, and infrastructure applications. Based on recent market forecasts, growth in silicon carbide sales outside of China should remain challenging before recovering in calendar 2026," notes Erickson. "We are well positioned in this market as we have a large customer base and are currently engaged in benchmarking efforts with multiple potential new silicon carbide customers around the globe, including in China. While we remain cautiously optimistic about the opportunities in China, we also recognize the geopolitical, trade and intellectual property risks associated with this market. Recently, we filed a lawsuit in China against a local supplier for intellectual property infringement. This action relates to features of products by that company targeted at wafer-level burn-in of silicon carbide devices that we believe infringe on Aehr's intellectual property and patents granted to Aehr by the Chinese patent office. Our current fiscal year forecast includes contemplated orders and revenue yet to be booked for silicon carbide wafer-level burn-in systems and WaferPaks destined for silicon carbide manufacturers in China. It is important to bring this to our shareholders attention, as recent trade-related developments in the US and the emergence of competitive offerings in China that we believe infringe on our intellectual property have heightened the risk associated with bookings and revenue from Chinese customers," he cautions.

Silicon carbide to comprise under half of full-year revenue

"As we look at the composition of our total revenue for this fiscal year, silicon carbide is expected to account for less than half our total revenue as we have seen our expansion into additional markets capture real market share gains. AI processors, including wafer-level and package parts, could comprise as much as 40% of our total revenue this fiscal year, up from effectively zero revenue last year. GaN, hard disk drives, silicon photonics integrated circuits, and other semiconductor package part revenues will comprise about another 20% of total revenue. We are not pivoting away from silicon carbide but rather are generating growth in these other markets while not seeing the growth in silicon carbide this year like we saw last year. According to recent market research from companies such as Yole, the estimated revenue for silicon carbide semiconductors in 2024 was around $2.5bn and is expected to reach $10bn by the end of the decade. To put this into perspective, the semiconductor market is projected to grow from about $600bn overall in 2024 to over $1 trillion by the end of this decade, so silicon carbide will be about 1% of the overall semiconductor market by 2030," Erickson notes.

"Aehr's innovative solutions are poised to capitalize on this growth in the overall semiconductor market by addressing the critical reliability needs of next-generation applications and leveraging key megatrends shaping the semiconductor industry. Reliability has become a critical priority across a wide range of industries, including combustion and electric vehicles, data centers, electrification of the world's infrastructure, and a wide range of AI applications. Factors such as smaller semiconductor geometries, the increasing adoption of compound and optical semiconductors, and the complexities of ensuring semiconductor reliability ever increasing power and

performance of semiconductors and advanced packaging are driving the demand for wafer-level and packaged part test and burn-in systems. Aehr's solutions are instrumental in reducing early operational failures and ensuring long-term device performance in these rapidly advancing markets," Erickson stresses. '

"With strong customer engagements, expanding market opportunities, and innovative products designed to meet evolving demands, we are optimistic as we move into the second half of our fiscal year and maintain our previously stated financial guidance for the fiscal year." For full-year fiscal 2025 (ending 30 May), Aehr expects revenue of at least $70m (up from $66.2m for full-year 2024) and non-GAAP net profit before taxes of at least 10% of revenue.

"Looking past quarterly variations to the full year and beyond, we are excited about the current and emerging market opportunities for our products, which not only position us for a successful fiscal year, but also lay a solid foundation for long-term, sustainable growth in the years ahead," Erickson concludes.

www.aehr.com

Aehr receives initial FOX-XP system order from GaN power semiconductor supplier

Aehr has received an initial production order from a top-tier automotive semiconductor supplier for a FOX-XP wafer-level test & burn-in system with fully integrated FOX WaferPak Aligner for production test of its gallium nitride (GaN) power semiconductor devices. The system was scheduled to ship immediately.

"We have been working closely with this customer for over a year to support their evaluation and qualification process for delivering GaN power semiconductor devices to their customers," notes president & CEO Gayn Erickson. "We are thrilled to receive this initial production purchase order, signaling their commitment to move forward with volume production wafer-level burn-in of their GaN devices on our FOX-XP platform," he adds.

"This customer has extensively utilized a FOX-NP system under an evaluation agreement for production qualification and reliability testing of their devices over the past year. As part of the evaluation, they purchased a significant number of our proprietary WaferPak full-wafer Contactors to successfully qualify a wide range of GaN device types designed for multiple end-use applications including industrial, solar, data center and automotive markets," Erickson continues.

"Our FOX-P platform allows customers using the FOX-NP for device qualification and reliability testing of power semiconductors like GaN and silicon carbide (SiC) to transition seamlessly to the FOX-XP multi-wafer fully automated system, which is capable of testing up to nine wafers in parallel and is specifically designed to handle high-voltage testing and high-temperature gate and drain stress test requirements. By leveraging our FOX-XP system and our proprietary WaferPak full-wafer Contactors, customers can easily test wafers of varying sizes from 6- to 12-inches by simply purchasing new WaferPaks, while utilizing the same FOX-XP system and FOX WaferPak Aligner."

"Like SiC, GaN semiconductor MOSFETs are wide-bandgap devices that offer significantly higher power conversion efficiency than silicon. GaN is particularly well suited for lower-power applications such as sub-1000W power converters (fast chargers) used in consumer electronics like cell phones, tablets and laptops. Additionally, it is increasingly being adopted for automotive power converters, supporting electrical systems in both electric and traditional gasoline-powered cars, as well as being targeted at data-center power applications where power efficiency and delivery are critical to support the massive amount of computing power and data storage being installed over the next decade. Along with the increased usage in automotive and data centers, many industry experts and analysts predict that GaN MOSFETs will eventually replace silicon as the preferred technology for power conversion in photovoltaic (solar panel) applications," says Erickson.

"We view GaN as a transformative and rapidly growing technology in the power semiconductor market. With an anticipated compound annual growth rate of more than 40%, the GaN market is projected to reach $2.5bn in annual device sales by 2029 according to Yole Group's Power SiC/GaN Compound Semiconductor Market Monitor. In addition, Frost & Sullivan estimates GaN semiconductors will account for over 10% of the worldwide power semiconductor industry by the year 2028. This represents a significant growth opportunity for Aehr's wafer-level test & burn-in solutions," he reckons.

Available with multiple WaferPak Contactors (full-wafer test) or multiple DiePak Carriers (singulated die/module test) configurations, the FOX-XP and FOX-NP systems are capable of functional test and burn-in/cycling of devices such as silicon carbide and gallium nitride power semiconductors, AI (artificial intelligence) processors, silicon photonics as well as other optical devices, 2D and 3D sensors, flash memories, magnetic sensors, microcontrollers, and other leading-edge ICs in either wafer form factor, before they are assembled into single- or multi-die stacked packages or in singulated die or module form factor.

METLEN investing in gallium production in Greece

Multi-national industrial and energy company METLEN Energy & Metals of Athens, Greece – which operates the only vertically integrated bauxite, alumina and primary aluminium production unit in the European Union (EU) with privately owned port facilities — says that the Metallurgy Committee, in a joint session with the Capital Allocation Committee, has made the final investment decision (FID) to proceed with implementing a €295.5m plan for the production of bauxite, alumina and gallium.

To be implemented in Agios Nikolaos, Viotia (within the historic 'Aluminium of Greece' plant), the project should significantly enhance the production capacity while incorporating gallium into industrial production for the first time.

The investment plan aims to achieve a total production capacity of 2 million tonnes of bauxite (annually), 1,265,000 tonnes of alumina (up from 865,000 tonnes currently), and 50 metric tonnes (Mt) of gallium for the first time. All three materials are included in the European Union's list of critical raw materials (CRMs). The total capital expenditure (CapEx) includes the following investments:

- development of research and new bauxite mining deposits;
- construction of new facilities and procurement of mechanical equipment for gallium production;
- new facilities and equipment for the expansion and modernization of alumina production capacity;
- energy supply infrastructure for the industrial unit;
- port expansion and upgrades;
- other road infrastructure and flood protection projects.

The investment "strengthens Europe's self-sufficiency in critical raw materials and bolsters Greece's strategic position on the global landscape. Moreover, it shields the European industry from external dependencies," says METLEN's chairman & CEO Evangelos Mytilineos. "We are proving our commitment to innovation, sustainable development and circular economy, while reaffirming METLEN's role as a leader in the transition toward greener and more resilient industrial production."

As a by-product of certain qualities of bauxite (including Greek bauxite) during the refining process into alumina, gallium production is almost entirely concentrated in China. However, China's decision in July 2023 to impose export restrictions on gallium highlighted the West's vulnerability and the need to diversify supply sources, says METLEN.

The firm adds that the investment enables Europe to completely substitute gallium imports, significantly bolstering its strategic autonomy and minimizing reliance on external suppliers. This autonomy is crucial for reducing dependence on third countries and ensuring the production of critical technologies across various sectors, from energy transition to defence, e.g. integrated circuits used in computing and telecoms, light-emitting diodes (LED) and permanent magnets etc.

The production of these three critical materials — valued at about €1bn — will be exported to European and North American markets.

The investment will also introduce new environmentally friendly technologies, reducing the facility's carbon footprint. In addition, through critical synergies with METLEN's Energy Sector, energy costs will become completely sustainable, says the firm.

METLEN has submitted the project under Greece's Strategic Investments Law. The investment also meets the criteria of the 'Temporary Crisis and Transition Framework' (TCTF), aimed at supporting the economy in the aftermath of the Russian invasion of Ukraine.

Furthermore, the project recently received the European Commission's STEP SEAL ('Sovereignty Seal'), recognizing its significant contribution to the EU's self-sufficiency in critical raw materials.

Completion of the works and production start-up is scheduled for 2026 for bauxite, with alumina and gallium production beginning gradually from 2027 and full-scale operation by 2028.

www.metlengroup.com

Neo completes sale of Rare Metals facility in Oklahoma

Co-founder Kevin Reading buys back gallium trichloride plant

Neo Performance Materials Inc of Toronto, Canada has completed the sale of its equity ownership interest in Neo Rare Metals (Oklahoma) LLC in Quapaw, OK, USA – which produces gallium trichloride – to the facility's general manager & co-founder Kevin Reading.

The purchaser acquired Neo's 80% equity stake in Quapaw for US$1.5m. The deal also includes a seven-year agreement for the purchase by Quapaw of gallium from Neo's recycling facility in Peterborough, Ontario, as well as for the processing and transfer of gallium scrap to the Peterborough recycling facility.

Completion of the transaction is a key step in Neo's operational transformation, as it continues to streamline its business globally and optimize its asset portfolio to support its long-term scale and growth ambitions.

"With the completion of this sale, Neo is well positioned to reinforce our core operations to maximize shareholder value," reckons Neo's president & CEO Rahim Suleman. "We look forward to continuing our partnership with the entrepreneurial owner-operator team at Quapaw."

www.neomaterials.com

Almae orders Riber GSMBE production system

Gas-source MBE to enhance production capabilities for ultra-high-speed InP photonic chips

Molecular beam epitaxy (MBE) system maker Riber S.A. of Bezons, France has received an order for a production MBE system from Almae Technologies SAS of Marcoussis, France — which was spun off in 2016 from III-V Lab of Palaiseau, France (the joint laboratory between Nokia, Thales and France's micro/nanotechnology R&D center CEA-Leti in Grenoble) — in order to enhance its production of photonic components addressing the growing demand in telecoms and datacoms markets for ultra-high-speed optical data transmission, driven by the surge in artificial intelligence (AI) applications requiring increasingly higher data volumes.

The new order continues a long-standing partnership, initiated with Riber's delivery of a gas-source MBE (GSMBE) system to Almae in 2019. Riber says that this underscores the reliability and relevance of its MBE solutions for manufacturing ultra-high-speed indium phosphide (InP) photonic chips, vital for next-generation datacom infrastructures and broader future connectivity solutions.

GSMBE is particularly well suited for the rigorous requirements of multi-epitaxy processes typical in photonic applications, which demand high machine stability, reproducibility and uniformity. Collaboration between Almae and Riber has driven significant productivity optimizations for GSMBE systems. By combining Almae's process expertise with Riber's technical know-how, advances have been achieved in system design, integrated instrumentation, and process control.

"Almae's ambition is to become a global leader in advanced photonic solutions for ultra-high-speed fiber-optic networks," says Almae's CEO Jean Louis Gentner. "Almae's development relies on innovative processes using GSMBE, providing our products with a differentiated competitive advantage in performance. Acquiring this new system marks an important milestone in developing our industrial platform and will significantly boost our productivity in a highly competitive market," he adds.

"This new order from Almae Technologies strengthens our strategic partnership established in 2017 and reflects the renewed confidence in our MBE solutions," comments Riber's chairwoman & CEO Annie Geoffroy.

www.almae-technologies.com

Teledyne Imaging Sensors places repeat order for Riber MBE 412 cluster system

TIS expands to three systems to fulfill added contracts for new high-performance IR devices

Long-standing US-based customer Teledyne Imaging Sensors (TIS) has placed a repeat order for a Riber MBE 412 cluster research system (for delivery in 2025) to expand its production capacity and fulfill additional contracts for manufacturing new high-performance infrared devices.

Following the order placed in July 2024, the latest order is said to strengthen the strategic relationship between Riber and Teledyne. Teledyne will now operate a fleet of three MBE 412 cluster systems dedicated to producing devices for infrared cameras used in space and terrestrial astronomy. Teledyne's solutions have contributed to over 48 space missions, highlighting their key role in space exploration.

Riber says that its automated MBE 412 cluster platform is specifically designed to meet the demands of advanced applications, particularly for growing MCT (mercury cadmium telluride) materials. It has an extremely low growth window of about 200°C, with uniformity variations of less than 1% on 7cm x 7cm samples. The combination of its unique geometry, advanced instrumentation capabilities, and Riber's Crystal XE software is said to ensure optimal performance for high-value components.

"This 40-year collaboration [with Teledyne Imaging Sensors], built on trust and excellence, serves as a model for us," comments Riber's president & CEO Annie Geoffroy. "As the first link in the value chain, we are honored to contribute to advancing cutting-edge technologies for space exploration," she adds.

"We are delighted to strengthen our partnership with Riber. Their MBE systems deliver outstanding performance, crucial for meeting the rigorous requirements of our space- and ground-based astronomy applications," comments Dr Michael Carmody, senior director of operations at Teledyne Imaging Sensors. "This long-standing partnership reflects our trust in their technical expertise and their ability to support our rapid capacity expansion."

www.teledyneimaging.com/en/aerospace-and-defense/products/sensors-overview

Veeco tightens revenue and EPS guidance ranges for fourth-quarter and full-year 2024

Forecasts raised for revenue but reduced for EPS

Epitaxial deposition and process equipment maker Veeco Instruments Inc of Plainview, NY, USA has revised its guidance for fourth-quarter 2024 revenue from $165–185m (forecasted in early November) to $175–185m (growing from $173.9m a year ago).

Revenue guidance for full-year 2024 has been narrowed from $690–730m (forecasted in August) to $710–720m (the midpoint of which also exceeds the midpoint of the original forecast of $680–740m, as well as being up 7.3% on full-year 2023).

Guidance for non-GAAP diluted earnings per share for fourth-quarter 2024 has also been tightened, from $0.35–0.45 (forecasted in early November) to $0.36–0.44 (down on $0.51 a year ago).

Likewise, guidance for full-year 2024 diluted EPS has been tightened from $1.65–1.85 (forecasted in August) to $1.69–1.76 (the midpoint of which is slightly below that of the original forecast of $1.60–1.90, but is still above full-year 2023's $1.69).

www.veeco.com

UCSB's Chris Van de Walle awarded APS' 2025 Aneesur Rahman Prize for Computational Physics

Award for development and application of first-principles methods for computing structural, electronic and optoelectronic properties of point defects and interfaces

Chris Van de Walle, a distinguished professor of materials at University of California Santa Barbara (UCSB), has been awarded the American Physical Society's 2025 Aneesur Rahman Prize for Computational Physics. Dating back to 1993, the prize honors Rahman, a founder of the field of molecular dynamics who pioneered computational methods for modeling physical systems.

Van de Walle is an elected member of the US National Academy of Engineering and a fellow of APS, the Institute of Electrical and Electronics Engineers, the American Association for the Advancement of Science, the Materials Research Society, and the American Vacuum Society.

Van de Walle performs computational work to develop a fundamental understanding of the physics and chemistry of materials in order to improve existing materials and discover new ones. His work on interfaces has assisted generations of semiconductor physicists in designing novel heterostructures, and his methodologies have helped to guide the development of devices such as transistors and lasers and, recently, the structures that underlie novel qubits. His research group's approaches in the area of point defects have been adopted by researchers throughout the world in a range of applications, from developing better materials for fuel cells to overcoming efficiency limits in light-emitting diodes.

UCSB's distinguished professor of materials Chris Van de Walle.

APS selected Van de Walle for the Rahman Prize in recognition of his "development and application of first-principles methods for computing the structural, electronic, and optoelectronic properties of point defects and interfaces."

The defects that used to be viewed as detrimental to materials have recently emerged as functional elements in quantum information science, and the techniques developed in Van de Walle's group are now employed to analyze and design quantum sensors and single-photon emitters.

"The Rahman Prize serves as a testament to his ability to identify and help solve critical challenges to technological applications, and it further demonstrates the global impact that his first-principle techniques and computational research have made," comments Umesh Mishra, dean of UCSB's College of Engineering.

Van de Walle acknowledged the contributions of many people, including mentors such as Richard Martin and Sokrates Pantelides, to the work recognized by the award.

Van de Walle received a Vannevar Bush Faculty Fellowship in 2022 from the US Department of Defense, a $2.5m award to study the processes that limit the efficiency of light-emitting diodes, lasers and other optoelectronic devices.

"I am also very grateful to the Materials Department, the College of Engineering, and the UC Santa Barbara campus for providing a supportive and stimulating environment for fundamental computational research," says Van de Walle.

https://news.ucsb.edu/2024/021663/materials-scientist-chris-van-de-

StratEdge partners with Vitale Engineering as manufacturer's representative for Upstate New York

Vitale to expand access to packaging technologies across industries such as aerospace, telecoms and defense

StratEdge Corp of Santee, near San Diego, CA, USA (which designs and makes packages and provides chip assembly & test services for microwave, millimeter-wave and high-speed digital devices) has appointed Vitale Engineering as its exclusive manufacturer's representative for Upstate New York. Vitale Engineering will expand access to StratEdge's packaging technologies across industries such as aerospace, telecoms and defense.

"Vitale Engineering's deep engineering knowledge and commitment to solving complex challenges make them an ideal partner," comments Casey Krawiec, StratEdge's VP of global sales. "Their ability to foster innovation and connect with clients in Upstate New York will help us better serve customers in this vital region."

Vitale Engineering specializes in providing tailored solutions for high-tech applications, leveraging decades of expertise in technical sales, product design, and project management. They support industries that demand precision and performance.

"This partnership allows us to deliver world-class semiconductor packaging solutions to clients who rely on advanced technologies to drive their success," says Vitale Engineering's president Adam Vitale. "Together, we are poised to address the challenges of high-frequency and high-power applications."

Vitale Engineering will represent StratEdge's full line of post-fired and molded ceramic semiconductor packages, which are designed for high reliability and extreme performance in demanding environments.

www.vitaleengineering.com
www.stratedge.com/packages.html

JST appoints new chief technology officer

Ismail Kashkoush to lead engineering, technology and product line teams in developing surface preparation products and processes

JST Manufacturing Inc of Meridian, ID, USA (a provider of wet benches, single-wafer surface preparation equipment and chemical processing systems) has appointed Dr Ismail Kashkoush as chief technology officer. Bringing over 30 years of engineering and industry expertise, he will lead JST's engineering, technology and product line teams in the development of its surface preparation products and processes.

Specifically, Kashkoush will oversee the development and strategy for JST's engineering teams in driving product advancement to support profitable growth. He will also introduce the company's products and technology globally and maintain the technology roadmap to support company growth objectives for all surface preparation and technology nodes requirements. Kashkoush will work with partners to lead new technology advancements and guide next-generation technologies that JST will bring to customers.

"Ismail brings a wealth of expertise, a fresh perspective and a transformative vision to our technology teams," says CEO Ryan Zrno. "As we amplify our commitment to technology innovation, Ismail will help us focus on delivering groundbreaking solutions to our clients, partners and key stakeholders."

Previously, Kashkoush was CTO for Akrion Technologies Inc, where he maintained its technology roadmap to support growth objectives for all FEOL/BEOL processes. As well as his patent portfolio, Kashkoush has many technical publications and conducted regular seminars on wafer surface preparation technology for the IC, MEMS, FPD and PV sectors. He earned a Ph.D. in Engineering Sciences from Clarkson University in 1993.

"I've spent my career understanding the technical challenges often plaguing customers within the wet processing space and look forward to bolstering innovative product and technology development during this pivotal time in JST's growth, showcasing JST's ability to address wide-ranging customer requirements with flexible technologies and top-notch service," says Kashkoush.

Kashkoush joins at a time when JST is seeing growth in single-wafer processing and batch processing across both silicon and compound semiconductor markets for key target applications including MEMS and sensors, optoelectronics, lasers, LEDs, and photodiodes. The rapid acceleration of artificial intelligence, Internet of Things, 5G and other emerging technologies will require accelerated development of advanced cleaning technologies to support the manufacturing of smaller, complex semiconductor devices, says the firm.

JST exhibited its full line of wet-processing solutions at electronica 2024 in Munich, Germany (12–15 November).

www.electronica.de/en
www.jstmfg.com

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Polar Light achieves 625nm-wavelength red pyramidal micro-LED

Fabrication on same material as green and blue micro-LEDs promises monolithic RGB integration

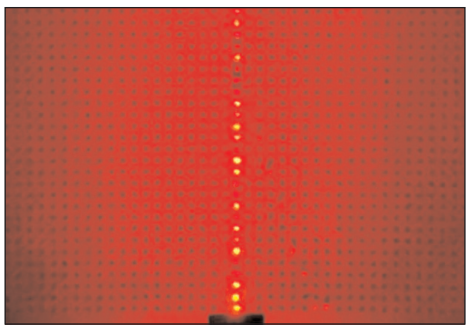
Polar Light Technologies (PLT) — which stems from research by founder professor Per-Olof Holtz and his team at Linköping University (with support from Sweden's innovation agency Vinnova) — has fabricated 625nm-wavelength red-light-emitting pyramidal micro-LED based on its non-etching bottom-up concept. The firm has hence achieved red, green and blue pyramidal micro-LEDs using the same material compound.

The pyramidal design has the ability to be manufacturable while maintaining what is said to be excellent micro-LED performance, laying the foundation for monolithic RGB displays, enabling spatial computing and next-generation panel displays.

Red without compromise

Blue and green micro-LEDs have been in the market for years, but reaching the red part of the spectrum has been difficult due to fundamental challenges in the material properties. There are several workarounds or alternatives for achieving red but they all come with some compromises, such as efficiency, manufacturability or the need to integrate with other material systems.

"Pursuing Polar Lights' innovative pyramidal LED concept has been



about overcoming those challenges without compromises," says chief technology officer Lisa Rullik. "We have succeeded in realizing the red-emitting micro-LEDs based on our innovative pyramidal structure."

Unique pyramidal structures

Polar Light Technologies' micro-LED is composed of pyramid shapes that are built with a novel bottom-up approach, a technology that is said to provide unique benefits:

- The inevitable strain in the lattice-mismatched indium gallium nitride (InGaN/GaN) structures is reduced, which is important to be able to make blue, green and red micro-LEDs with the same material system, i.e. to fabricate monolithic RGB.
- It gives a unique possibility to integrate the frontplane with a backplane.
- No etching is needed, which means that performance is maintained also for smaller dimensions since no etching damage occurs. It also enables even sub-μm LEDs, i.e. nano-LEDs.
- It is easier to manufacture and integrate with CMOS and TFT
- The emission cone is narrow: there is a Lambertian light lobe from the emitter, which is important for micro-projectors.

Polar Light says that, with these unique benefits, its micro-LEDs solve key challenges in bringing the technology to the market.

Performance, manufacturability and nano-LEDs

Polar Light claims that its same-compound-based micro-LEDs offer high performance and excellent manufacturability, as well as very small dimensions and a narrow emission cone. The technology also opens up nano-LED applications — as soon as the rest of the display technology catches up.

"Our technology addresses micro-LED challenges in a way that has never been done before," claims CEO Oskar Fajerson. "Now we're moving towards commercialization of this groundbreaking technology, focusing on putting products on the market."

www.polar-light-technologies.com

Porotech & Foxconn advance partnership from R&D to mass production of AR and micro-LED technology

Pixel size reduced to 1.25μm, forming process platform to be applied in Q4/2025

Hon Hai Technology Group (Foxconn) of Taipei, Taiwan (the world's largest electronics manufacturer and technology service provider) has entered the augmented reality (AR) glasses market by partnering with fabless micro-LED company Poro Technologies Ltd (a spin off from the Cambridge Centre for Gallium Nitride at the UK's University of Cambridge that has developed porous GaN material and has an R&D center in Hsinchu, Taiwan). The firms will leverage Porotech's gallium nitride (GaN) technology and Foxconn's vertical integration capabilities to develop micro-LED display technology and AR applications.

In early 2024, Porotech officially announced a strategic collaboration with Foxconn, Taiwanese foundry Powerchip Semiconductor Manufacturing Corp (PSMC) and Taiwan-based integrated touch and display module company General Interface Solution Holding Ltd (GIS, in which Foxconn has a stake) to build what is said to be the industry's first 8-inch platform for micro-LED applications. Before the end of 2024, the partnership achieved a breakthrough in reducing pixel size to 1.25μm. Laying the critical foundation for the mass production of micro-LEDs, this platform is set to be applied in 2025, further advancing the development and commercialization of high-spec micro-LED products, including AR glasses and high-resolution displays.

Foxconn's micro-LED facility in Taichung, Taiwan.

"The collaboration with Foxconn, PSMC and GIS in 2024 is a significant technological milestone and a testament to our commitment to accelerating the commercialization of micro-LED technology," says Porotech's CEO Dr Tongtong Zhu. "Completing the 1.25μm process platform at year-end provides groundbreaking technical support for high-performance display products," he adds. "We look forward to these technological achievements bringing new value to AR glasses and global technology as a whole."

Porotech believes that, by combining Foxconn's vertical integration advantages, PSMC's manufacturing expertise and GIS's capabilities in display technology integration, the establishment of this processing platform and technological breakthroughs will further solidify micro-LED technology's market position in AR and high-performance display sectors. "We are committed to developing lighter, thinner, and higher-performance miniaturized display solutions to meet the demands of next-generation display technologies in the future," says the firm.

Foxconn plans to establish a micro-LED wafer processing line in Taichung, Taiwan, with mass production starting in fourth-quarter 2025. The new plant is expected to position Taiwan as a critical hub for AR glasses and micro-LED technologies.

www.porotech.co.uk
www.foxconn.com
www.powerchip.com
www.gis-touch.com

SemiLEDs' revenue falls slightly in December quarter

Margins rebound as losses cut further

For its fiscal first-quarter 2025 (to end-November 2024), LED chip and component maker SemiLEDs Corp of Hsinchu, Taiwan has reported revenue of $1.261m. This is down from revenue of $1.324 last quarter and $1.65m a year ago.

Gross margin rebounded from 12% last quarter to 21%, up on 15% a year ago. Operating margin has recovered from −62% to −52%, almost matching −50% a year ago.

Net loss has been cut further, from $598,000 ($0.12 per diluted share) a year ago and $560,000 ($0.08 per diluted share) last quarter to $547,000 ($0.08 per diluted share).

Cash and cash equivalents have fallen further, from $2.322m a year ago and $1.671m at the end of last quarter to just $1.248m at the end of November.

www.semileds.com

Aledia makes available micro-LED technology for immersive AR applications

At the Consumer Electronics Show (CES 2025) in Las Vegas (7–11 January), Aledia S.A of Echirolles, near Grenoble, France (a developer and manufacturer of 3D micro-LEDs for display applications based on its large-area gallium nitride nanowires-on-silicon platform) announced the availability of its micro-LED technology for augmented reality applications and next-generation displays for vision applications.

Tech giants are releasing prototypes and targeting commercial launches of micro-LED-based smart glasses as early as 2027. While AI-powered use cases for AR have emerged over the last year, critical hardware challenges — power consumption, bulkiness and manufacturing costs — remain significant barriers to mass adoption, notes Aledia.

After 12 years of R&D, a portfolio of nearly 300 patents and $600m in investment, Aledia reckons that its micro-LED-based micro-display — with red, green and blue micro-LEDs grown monolithically on the same substrate –can solve the toughest hardware challenges, paving the way for immersive, AI-powered AR vision.

"Immersive technologies such as AR haven't reached their full potential as the industry has yet to design screens that are both slick and highly functional," says president & CEO Pierre Laboisse. "We've created a nanowire technology that makes micro-LED displays thinner, more power efficient and easier to produce for mass adoption. By next CES, OLED and LCOS will already be phased out in favor of our superior micro-LED technology," he reckons.

Aledia's micro-LED platform for AR

Aledia says that its micro-LED technology based on 3D gallium nitride (GaN) on silicon nanowires opens the way to next-generation smart displays:

- The technology is said to deliver enhanced brightness and energy efficiency compared with 2D LEDs, along with superior pixel density and resolution. The 3D structure allows precise and directive light emission, making Aledia's displays highly efficient and suited to advanced applications such as AR. During R&D testing, the nanowires improved directivity and light efficiency in real-world settings, which are crucial for immersive AR experiences.
- Aledia's hybrid bonding technology combines micro-LED and driver electronics into what is claimed to be the smallest chip on the market, resulting in thinner displays and superior power efficiency for longer battery life.
- Aledia's $200m in-house pilot production line in Europe's 'Display Valley' enables faster iteration without initial volume constraint. By utilizing semiconductor-grade silicon in 8-inch and 12-inch formats, it lowers production costs for large-scale production of micro-LEDs, accelerating widespread adoption in a wide range of displays. Aledia is able to support customer demand ramp up to nearly 5000 wafer starts per week.

"Our Champagnier factory is a key milestone for European innovation, and we are proud to represent it at the Auvergne Rhône-Alpes Pavilion at CES," says Laboisse. "We are redefining global standards of display technology with our efficient and high-performing chips, positioning Grenoble as the global center of micro-LED production."

www.ces.tech
www.aledia.com

VueReal appoints VP of semiconductor engineering

Micro-LED technology firm VueReal Inc of Waterloo, ON, Canada has appointed Giuseppe Buscemi as VP of semiconductor engineering. The firm reckons that, due to his extensive experience in semiconductor production facilities and deep knowledge of micro-LED technology, he will be pivotal in scaling its cartridge production capabilities to meet growing demand.

In semiconductor manufacturing, Buscemi has overseen complex production processes, optimized yield, and ensured the delivery of high-quality products at scale. His track record in navigating the challenges of scaling production aligns with VueReal's aim to expand its MicroSolid Printing Platform and to advance its position in the micro-LED display and device industry.

"His unparalleled expertise in semiconductor engineering and production and his in-depth understanding of micro-LED technology will be instrumental as we move into this critical growth phase," reckons CEO Dr Reza Chaji. "Giuseppe's leadership will help us meet the increasing demand for our innovative products while maintaining the highest standards of quality and efficiency."

Buscemi will lead efforts to optimize manufacturing processes, expand production capacity, and develop solutions that ensure seamless integration of VueReal's technology into customer applications. The firm reckons that his strategic insights and technical acumen will strengthen its ability to deliver scalable and sustainable micro-LED solutions across various industries.

"VueReal's innovations in micro-LED technology are shaping the future of displays and sensing applications, and I am eager to contribute to scaling our production to bring these groundbreaking solutions to a wider market," says Buscemi.

www.vuereal.com

Plessey and Meta develop brightest red micro-LED display for augmented reality glasses

Up to 6,000,000nits at sub-5µm resolution with ultra-low power consumption

Plessey Semiconductors Ltd of Plymouth, UK — which develops embedded micro-LED technology for augmented-reality and mixed-reality (AR/MR) display applications — and Meta Platforms Inc have developed what is claimed to be the brightest red micro-LED display suitable for AR glasses. Offering up to 6,000,000nits at high resolution (<5_m) with ultra-low power consumption, it is reckoned to overcome critical technical challenges, helping to pave the way for the next computing platform.

The achievement follows Meta recently unveiling Orion, its true AR glasses prototype. This is said to combine the look and feel of a regular pair of glasses with the immersive capabilities of AR due to features such as its 70° field of view, silicon carbide high-performance waveguides, custom silicon, micro-LED projectors, and integrated input system.

As part of its long-term commercial agreement, Plessey is continuing to work with Meta by dedicating its manufacturing operations to support the development of prototypes and new technologies for potential use in the XR category.

"These types of breakthroughs are crucial to build AR glasses that help people stay more present and empowered in the world with a form factor people actually feel comfortable wearing," says Jason Hartlove, VP of display & optics, Meta's Reality Labs. "Our work with Plessey has pushed the boundaries of what's previously been possible, and it's only the beginning," he adds.

"The collaboration between Meta and Plessey has delivered a major breakthrough in the development of AR technology," reckons Plessey's CEO Dr Keith Strickland. "With the world's brightest red micro-LED display, we are one major step closer to making AR glasses a mainstream reality."

www.plesseysemiconductors.com/products/microleds

www.meta.com/en-gb/blog/quest/

Thorlabs acquires strategic partner Praevium Research

Vertically integrated photonics product maker Thorlabs Inc of Newton, NJ, USA has acquired Praevium Research Inc of Goleta, CA, USA, which was founded by Dr Vijay Jayaraman in 2001 and develops high-speed tunable vertical-cavity surface-emitting lasers (VCSELs). The two firms have been working together since 2008, when Praevium became a member of Thorlabs' Strategic Partner Program.

Over the past 17 years, Praevium has partnered with Thorlabs on the development and commercialization of several novel technologies, including the MEMS-VCSEL Swept-Wavelength Laser Sources, Swept Source OCT Systems at 1060nm and 1300nm, and broadband SLD Light Sources for OCT applications.

"Praevium's expertise and innovation in high-speed tunable MEMS-VCSEL laser design and fabrication has been instrumental to our success in bringing innovative lasers to the optical coherence tomography (OCT) medical device market and enabling our own OCT product lines," comments Thorlabs' president Jenn Cable. "I look forward to using our combined expertise to accelerate product development and commercialization."

"Thorlabs has been a fantastic partner for nearly two decades, and we have been honored to work with them to develop advanced laser technology that is improving the quality of human life across the globe," says Praevium's founder Vijay Jayaraman. "We are excited to join this world-class organization and multiply the impact of MEMS-VCSELs and other emerging photonics technologies across a broad variety of biomedical, sensor and other applications."

As a division of Thorlabs, Praevium will maintain its existing leadership, with Christopher Burgner as its general manager and Vijay Jayaraman as a senior scientist. It will continue to conduct business under the Praevium Research name operating out of its existing facility a short distance from Santa Barbara, CA, and maintain its focus on developing novel semiconductor lasers and detectors in partnership with the Thorlabs team in Jessup, MD.

www.praevium.com
www.thorlabs.com

Lynred launches Eyesential SW shortwave IR sensor

Lynred of Grenoble, France — which designs and makes infrared (IR) sensors for aerospace, defense and commercial applications — has launched Eyesential SW, its latest VGA-format shortwave infrared (SWIR) sensor for machine vision. Designed to offer the ideal cost-performance ratio for visible-like imaging to address specific performance needs in machine vision, Eyesential SW is said to have the performance and features sought by industry but at half the price of comparable IR sensors on the market. It also includes specific functions for spectroscopy applications, such as spectral line selection/deselection.

Featuring a high frame rate (300Hz full frame/1200Hz ¼ full frame) and what is claimed to be leading-edge performance in sensitivity and low noise, Eyesential SW is suited to the automation and data exchange trends in Industry 4.0 manufacturing, which require enhanced detection capabilities and improved real-time detection on production lines.

"Lynred's latest innovation, Eyesential SW, strikes the right balance between performance and cost for machine vision," says Pierre Jenouvrier, cooled product division director at Lynred. "This SWIR sensor puts an end to the dilemma of equipment makers having to compromise on performance or price," he adds. "The integrity of our InGaAs [indium gallium arsenide] technology, underpinning Eyesential SW and focusing on affordability, will give customers a new level of cost-effective VGA-format SWIR sensors which better address machine vision market demands."

Through Eyesential SW, a 640x512, 10µm-pitch SWIR (0.9–1.7µm) sensor with 14-bit digital output and COTS (commercial off-the-shelf) packaging, Lynred aims to bolster Europe's supply chain in SWIR sensors as well as strengthen its global offering in the machine vision market. The new sensor complements Lynred's SWIR product portfolio, which includes Snake SW (640x512/15µm), dedicated to high-end machine vision applications, and its recently acquired NIT SWIR modules.

Machine vision, scientific imaging and spectroscopy

SWIR wavelengths are able to pass through many solid materials, including silicon. Distinguishing materials and detecting humidity make them suitable for on-line industrial inspection and non-destructive control. Due to these key characteristics, Eyesential SW has many industrial applications, such as recycling operations to sort different types of plastics at high speed. Due to its sensitivity, high frame rate and capacity to select/deselect spectral lines, the SWIR sensor is also well suited to infrared spectroscopy, an application for identifying and quantifying almost any chemical species and for scientific imaging.

In the kit that Lynred offers to operate Eyesential SW are an electronic board, including mechanical and optical interfaces (C-Mount), and the Lynred Software Toolbox.

Eyesential SW was on display at SPIE Photonics West 2025 in San Francisco, CA, USA (28–30 January).

www.lynred.com

NUBURU announces board and committee appointments

Size of board increased from four to six

NUBURU Inc of Centennial, CO, USA — which was founded in 2015 and develops and manufactures high-power industrial blue lasers — has increased the size of its board of directors from four to six with the appointment of Dario Barisoni and Shawn Taylor for a term expiring at the 2025 annual meeting of shareholders (or until a respective successor is duly elected and qualified). They will also each serve on the board's Audit Committee.

Barisoni will also serve on the board's Nominating and Corporate Governance Committee and Taylor will serve on the Compensation Committee. He has over two decades of expertise in the technology sector, with a focus on optoelectronics, electronics and international business. His career spans senior leadership roles across Europe, the Middle East, and Asia, with a track record in market expansion, mergers & acquisitions, internationalization, and establishing international joint ventures and partnerships.

Barisoni has served as co-founder & managing director of Bionexus (a start-up with a focus on mergers & acquisitions in the healthcare sector) since 2024, and managing partner of 2Invest (an investment company with focus in the energy, technology, IT sectors and financial services) since 2023. Previously, from 2012 to 2023, he served as CEO Middle East & Asia to SIAE Microelectronica. As regional CEO, Barisoni established and expanded several subsidiaries across Asia and the Middle East, led multi-million-dollar telecom infrastructure projects, spearheaded sales & business development for Aisa and the Middle East, and led legal, financial, operational, sales and human resources departments.

Prior to this role, he has held executive positions for a range of European-based technology manufacturing companies including Germany's Rohde & Schwarz, Marconi plc and Pirelli Cables and Systems (now Prysmian). Barisoni has also served as a board member of the Italian Business Council UAE (a Dubai organization that associates all of the Italian enterprises operating or doing business in the country) since 2021; and as a board member of the Italian Chamber of Commerce to South East Asia since 2009. Barisoni holds an Executive MBA from POLIMI Graduate School of Management in Milan, Italy, and a Master of Science in Optoelectronic Engineering from Politecnico di Milano.

Taylor is a seasoned fractional chief financial officer with over 20 years of experience in SaaS technology, media, and high-value intellectual property sectors.

With a track record in both start-up and scale-up environments, he has played pivotal roles in venture capital-funded and publicly traded companies. His expertise encompasses corporate finance, initial public offerings, equity and debt financings, strategic restructurings, and merger & acquisition transactions. He has served as chief financial officer for a range of Europe-based entities including Eight Capital Partners plc, an international financial services operating company, since December 2023.

Prior to working with Eight Capital Partners, Taylor served as chief financial officer for the following companies: Bolt Global Media Ltd from August 2022 to December 2023; Quickmove Ltd. from January 2021 to February 2022; Gibbs Hybrid Ltd from August 2019 to December 2020; and Abal plc (formerly Imaginatik plc) from August 2005 to August 2019. Career highlights include spearheading the IPO of Imaginatik on the London Stock Exchange's AIM market, scaling businesses to significant revenue growth and negotiating high-value trade sales. He has been a fellow of and is a Chartered Accountant with the Institute of Chartered Accountants in England and Wales since 1990. Taylor has a BSc in Geography from Kings College, London University.

NUBURU regains compliance with NYSE American

NUBURU has been notified by NYSE American Market that it has resolved the deficiencies identified by it on 18 November 2024 (relating to NUBURU having an insufficient number of independent directors), and NUBURU is now compliant with NYSE American Market's continued listing standards.

www.nyse.com/markets.nyse-american

www.nuburu.net

Netherlands launches ChipNL Competence Centre to drive semiconductor innovation

Applications focus on manufacturing equipment, chip design, integrated photonics, quantum and heterogeneous integration

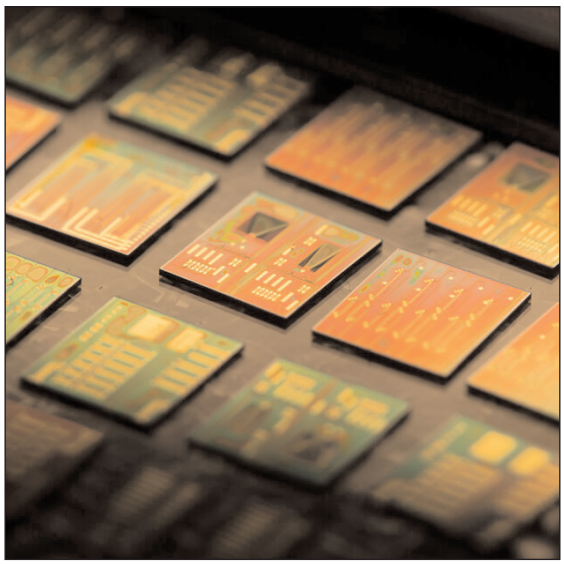
The ChipNL Competence Centre has been launched, aiming to advance technological capabilities and foster innovation in the Dutch semiconductor ecosystem. The European Commission and the Rijksdienst voor Ondernemend Nederland (RVO) have jointly allocated a budget of €12m for the next four years. Specifically, the four-year project aims to stimulate innovation, collaboration and talent development and to enhance global competitiveness of the Netherlands and Europe in semiconductor technologies.

The ChipNL Competence Centre is part of the European Chips Act. Within this, the European Competence Centres function as national hubs for research, development and cooperation between industry, government and knowledge institutions. They should contribute to accelerating innovation and technological solutions, stimulating talent development and strengthening the European value chain in semiconductors.

Dutch contribution to European network of Competence Centers

The ChipNL Competence Centre is a collaboration between Brainport Development, ChipTech Twente, High Tech NL, TNO, JePPIX, imec and the regional development companies OostNL, BOM and InnovationQuarter. It focuses on supporting and connecting parts of the value chains with Dutch SMEs, start-ups and scale-ups in the semiconductor sector and related application markets with a focus on semiconductor manufacturing equipment, chip design, (integrated) photonics, quantum and heterogeneous integration.

JePPIX (Joint European Platform for Photonic Integration Components and Circuits, an association of commercial enterprises, research



organizations and universities serving as a platform for promoting integrated photonics on a European level) is coordinated by TU/e.

In the ChipNL Competence Centre, TU/e brings its experience with managing the developer community for photonic integrated circuits from JePPIX, complementing Dutch electronic chip design capabilities with the latest photonic and heterogeneous techniques.

Activities and support of ChipNL Competence Centre

The ChipNL Competence Centre supports SMEs, startups and multinationals to access European pilot lines that allow them to test and validate new technologies in a controlled and advanced environment. In addition, an innovative design platform is being developed within the EU Chips Act to support industry in designing and developing customized semiconductor solutions. The ChipNL Competence Centre also facilitates access to this by providing support and knowledge. TNO, imec and JePPIX will be responsible for these activities.

To train the right talent for the future, the Centre will cooperate with the EU Skills Initiatives and the Microchip Talent reinforcement plan (project Beethoven). The talent program aims to promote the development of new skills and strengthen the labor market for the semiconductor sector. Brainport Development and ChipTechTwente will be responsible for these activities.

In addition, the ChipNL Competence Centre offers support in obtaining funding through the EU Chip Fund, which was set up specifically to stimulate innovative projects in the semiconductor industry. These activities are complemented by support in business development, fundraising and internationalization, as well as identifying innovation opportunities within the sector. The regional development organizations OostNL, InnovationQuarter and BOM and High Tech NL will be responsible for these activities.

The ChipNL Competence Center should further position the Netherlands as a hub for semiconductor innovation, while contributing to broader European goals.

Boost for Dutch SMEs and startups in the semiconductor industry

The grant aims to enable further support for the Dutch chip industry to strengthen its knowledge position and competitiveness and further consolidate its position within Europe. By supporting companies with access to pilot lines, the design platform, financing opportunities and talent programs, the ChipNL Competence Centre aims to provide a foundation for SMEs and startups to compete in the global market.

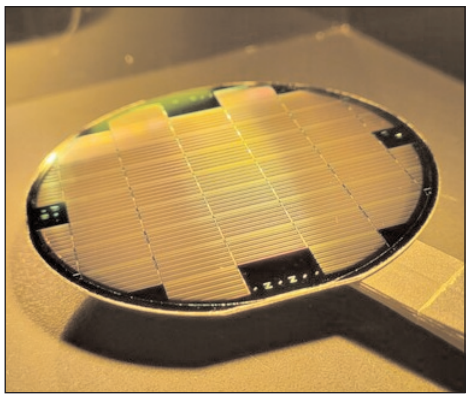
https://commission.europa.eu/strategy-and-policy/priorities-2019-2024/europe-fit-digital-age/european-chips-act_en

Ortel transfers C-band high-power cw laser from Emcore fab to Canadian Photonics Fabrication Centre

Customer samples due in February for fully qualified production devices in second-quarter 2025

Ortel LLC of Alhambra, CA, USA (which was acquired by Photonics Foundries in 2023, and offers products for wireless, sensing, satcoms and broadband applications) has transferred wafer fabrication for its flagship C-band, high-power, continuous wave laser module platform to pure-play III–V semiconductor wafer foundry Canadian Photonics Fabrication Centre (CPFC), which is located at the National Research Council of Canada. Transfer assures uninterrupted wafer supply and a smooth transition of the laser to expanding markets including LiDAR, fiber-optic sensing, coherent and externally modulated fiber-optic communications, and test & measurement.

The laser features a narrow linewidth (typically 50kHz), high power (up to 100mW) and low-noise performance. The laser is also available for DWDM applications as it is offered on the ITU wavelength grid. It is offered as the model 1790 in 14-pin butterfly form, model 1995 in a cooled TO56 package, and on various standard or custom chip-on-sub mount forms. Initial customer samples will be available in February, with fully qualified production device availability expected in second-quarter 2025.



Ortel C-band, high-power cw laser module featuring narrow-linewidth, high-power and low-noise performance.

"Throughout the design and qualification process, we've been thrilled to partner with the team at the CPFC," comments Grant Olecko, Ortel's VP of product line management. "Their wafer fab is a state-of-the-art facility offering key advantages over the prior Emcore fab including supply security, custom epitaxy growth, superior technology, and major capacity improvements. The CPFC's impressive world-class scientists and engineers leverage sophisticated tools and advanced process technology to help our customers achieve exceptional precision and optimized laser performance. These capabilities, layered with Ortel's recognized strengths in device design, vertical integration and global expertise, create a considerable advantage for customers," he adds.

The CPFC hosts a comprehensive toolset for commercial production of photonic chips including custom epitaxy growth services. Since 2004 it has accrued expertise in fabricating semiconductor lasers, optical amplifiers, high-speed modulators, micro-LEDs, and gallium nitride (GaN) RF ICs.

"We are delighted to formalize our long-term relationship with Ortel," says CPFC's director general Velko Tzolov. "This partnership will allow us to work together on innovative technologies that drive impactful device performance improvements while continuously maintaining highly reliable wafer fabrication."

www.ortel.com/sensing.html
https://nrc.canada.ca/en/

ROHM samples 1kW-class high-power IR laser diode

125W x 8-channel high-power array improves measurement distance and resolution in LiDAR applications

Japan-based ROHM has developed the RLD8BQAB3 high-output laser diode for use in ADAS (Advanced Driver Assistance Systems) equipped with LiDAR for distance measurement and spatial recognition. In addition to automotive applications, the firm is also initially supplying samples targeting consumer applications (drones, robot vacuums, golf rangefinders) and industrial applications (AGVs, service robots, and 3D monitoring systems such as sensors for human/object detection).

LiDAR has seen growing adoption in recent years across applications that require automation such as automotive ADAS, AGVs, drones, and robot vacuums, facilitating precise distance measurement and spatial recognition, notes ROHM. To detect information at greater distances with more accuracy, there is a need for laser diodes that serve as light sources to achieve high kW-level output while allowing multiple light sources to emit light at close intervals, the firm adds.

ROHM has established proprietary patented technology that achieves the narrow emission width of lasers, enhancing long-distance, high-accuracy LiDAR, beginning with the commercialization of the 25W output RLD90QZW5 in 2019 and the high-power 120W RLD90QZW8 in 2023. Building on these, the firm has developed a new 125W 8-channel (1kW-class) array-type product that meets the demand for a high-output, high-performance laser diode.

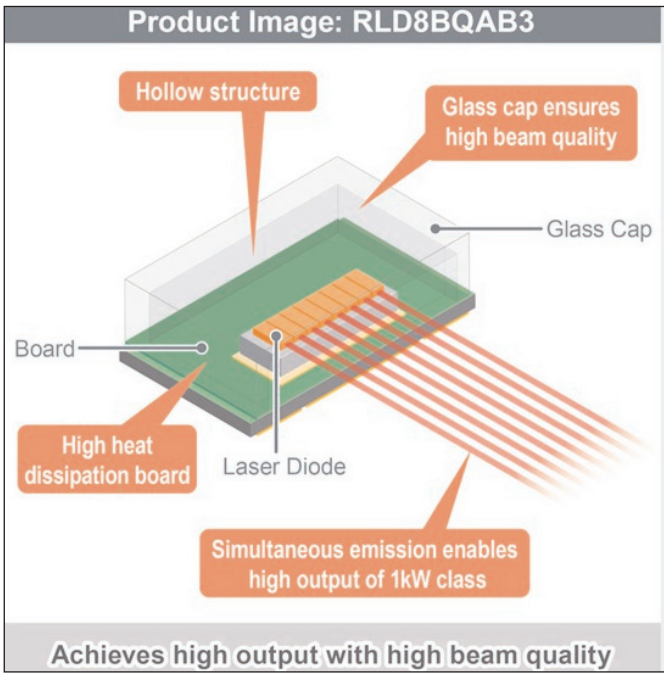
The RLD8BQAB3 is an ultra-compact surface-mount high-output 125W x 8-channel infrared laser diode for LiDAR applications that use 3D time-of-flight (ToF) systems to carry out distance measurement and spatial recognition. The optimized design features eight emission areas (each 300μm wide) per element, installed on a submount affixed to a high-heat-dissipation substrate.

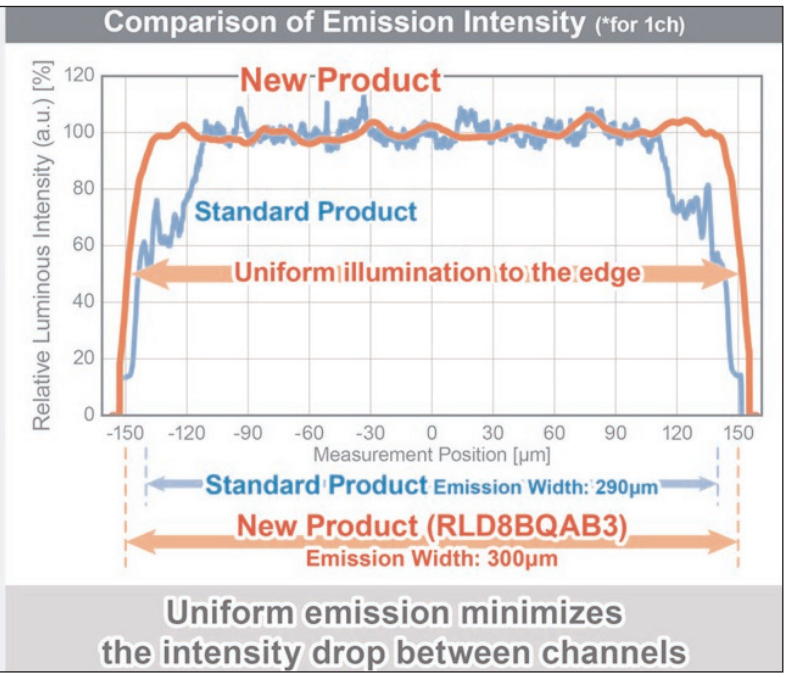
The package's emitting surface incorporates a clear glass cap — claimed to be an industry first for a surface-mount laser diode — eliminating the risk of light scattering caused by scratches during dicing that tends to occur with resin-encapsulated products, ensuring high beam quality. Each emission area is wired with a common cathode, enabling the selection of the irradiation method based on application needs — ranging from individual emission that increases the number of light-emitting points to what is claimed to be industry-leading simultaneous emission at ultra-high outputs of 1kW class.

The new product retains the key features of ROHM's conventional laser diodes

The new product retains the key features of ROHM's conventional laser diodes, including uniform emission intensity across the emission width along with a low wavelength temperature dependence of 0.1nm/°C (versus 0.26–0.28nm/°C for standard products). In addition, the array configuration narrows the regions of reduced emission intensity between channels, while the bandpass filter minimizes the effects of ambient light noise from the sun and other sources, contributing to long-distance detection and high-definition LiDAR.

www.rohm.com/products/laser-diodes/high-power-lasers/rld8bqab3-product





Voyant launches FMCW LiDAR sensor on a chip

Low-cost 4D LiDAR sensor enabled by integrated silicon photonic chip

Light detection & ranging (LiDAR) solution provider Voyant Photonics of Long Island City, NY, USA has announced the availability of the CARBON frequency-modulated continuous wave (FMCW) LiDAR sensor, featuring what is claimed to be the first truly effective and affordable LiDAR on a chip with solid-state beam steering.

Developed to revolutionize machine perception capabilities in industrial, robotics and security applications, the low-cost 4D LiDAR sensor's highly integrated silicon photonic chip is fingernail-sized and provides high-resolution, millimeter precision, object detection and static/dynamic segmentation up to 200m, at a fraction of the cost of existing best-in-class LiDAR makers, it is claimed.

Voyant says that it has achieved this performance and affordability by integrating optics on a LiDAR photonic integrated circuit (PIC).

Instant identification of moving objects

Unlike time-of-flight (ToF) LiDAR, FMCW LiDAR enables instant velocity at each point on top of traditional distance, reflectivity and intensity measurement. This provides '4D' capability: providing high-fidelity point cloud data with unparalleled accuracy, to give applications a true real-time view of their environment, up to 20 times per second. Instant velocity also enables vehicle to have ego-positioning capabilities, which is extremely efficient in GPS-denied environments and potentially makes a high-end inertial measurement unit (IMU) substitutable.

Operation in all weather conditions, and immune to retroreflective objects

CARBON is claimed to outperform best-in-class ToF LiDAR in operating through dust, fog, rain and snow, as well as being immune to sunlight interference – most notably at sunrise and sunset. The technology is also invulnerable to highly reflective objects, particularly retroreflectors (such as street signs, traffic cones, and safety vests), that suffer from blooming, blinding legacy ToF LiDARs.

Despite weighing just 250g, the compact-size CARBON is robust, with IP67 dust and water protection, with strong shock and vibration endurance. In addition, the low power required by FMCW laser technology ensures eye safety.

High-resolution, wide-angle and long-range

CARBON's high resolution of native 128 lines per frame provides camera-level resolution and, coupled with instant velocity measurement, it enables highly accurate detection and tracking of moving objects up to 200m away. The field of view is 45° vertical and 90° horizontal. Maximum detectable radial velocity is 63m/s (140mph). The sensor's software-defined LiDAR (SDL) allows users to modify the frame rate and adjust the field of view during operation, to focus on a zone of interest when and where it is needed and make any small object detectable and classifiable.

Voyant demonstrated CARBON at the Consumer Electronics Show (CES 2025) in Las Vegas

The CARBON LiDAR is available for order now, at $1490 for single units, with volume pricing available, and a two-year warranty.

www.voyantphotonics.com

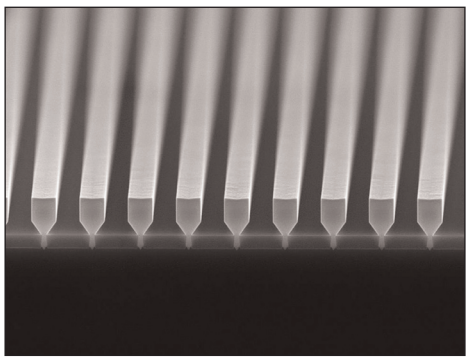
imec reports first full wafer-scale fabrication of electrically pumped GaAs-based nano-ridge lasers on 300mm silicon

Lasing at ~1020nm with 5mA threshold current, 0.5W/A slope efficiency and 1.75mW optical power show scalable path to high-performance silicon-integrated light sources

Nanoelectronics research center imec of Leuven, Belgium has demonstrated electrically driven gallium arsenide (GaAs)-based multi-quantum-well nano-ridge laser diodes fully, monolithically fabricated on 300mm silicon wafers in its CMOS pilot prototyping line. Achieving room-temperature continuous-wave lasing with threshold currents as low as 5mA and output powers exceeding 1mW, the results are said to demonstrate the potential of direct epitaxial growth of high-quality III–V materials on silicon ('GaAs nano-ridge laser diodes fully fabricated in a 300mm CMOS pilot line', Yannick De Koninck et al, Nature, volume 637, pages 63–69 (2025)). imec reckons that this provides a pathway to the development of cost-effective, high-performance optical devices for applications in data communications, machine learning and artificial intelligence.

The lack of highly scalable, native CMOS-integrated light sources has been a major roadblock for the widespread adoption of silicon photonics, notes imec. Hybrid or heterogeneous integration solutions (such as flip-chip, micro-transfer printing or die-to-wafer bonding) involve complex bonding processes or the need for expensive III–V substrates which are often discarded after processing. This not only increases costs but also raises concerns about sustainability and resource efficiency. The direct epitaxial growth of high-quality III–V optical gain materials selectively on large-size silicon photonics wafers hence remains a highly sought-after objective.

The large mismatch in crystal lattice parameters and thermal expansion coefficients between III–V and silicon materials inevitably initiates the formation of crystal misfit defects, which are known to deteriorate laser performance and reliability. Selective-area growth (SAG), combined with aspect-ratio trapping (ART), significantly reduces defects in III–V materials integrated on silicon by confining misfit dislocations within narrow trenches etched in a dielectric mask.



Scanning electron micrograph of a GaAs nano-ridge array after epitaxy.

"Over the past years, imec has pioneered nano-ridge engineering, a technique that builds on SAG and ART to grow low-defectivity III–V nano-ridges outside the trenches. This approach not only further reduces defects but also enables precise control over material dimensions and composition," says imec's scientific director Bernardette Kunert. "Our optimized nano-ridge structures typically feature threading dislocation densities well below $10^5 cm^{-2}$. Now, imec exploited the III–V nano-ridge engineering concept to demonstrate the first full wafer-scale fabrication of electrically pumped GaAs-based lasers on standard 300mm silicon wafers, entirely within a CMOS pilot manufacturing line," she adds.

Leveraging the low-defectivity GaAs nano-ridge structures, the lasers integrate InGaAs multiple quantum wells (MQWs) as the optical gain region, embedded in an in-situ doped p-i-n diode and passivated with an InGaP capping layer. Achieving room-temperature, continuous-wave operation with electrical injection is a major advancement, claims imec, overcoming challenges in current delivery and interface engineering. The devices show lasing at ~1020nm with threshold currents as low as 5mA, slope efficiencies up to 0.5W/A, and optical powers reaching 1.75mW, showcasing a scalable pathway for high-performance silicon-integrated light sources.

"The cost-effective integration of high-quality III–V gain materials on large-diameter silicon wafers is a key enabler for next-generation silicon photonics applications," reckons Joris Van Campenhout, Fellow Silicon Photonics & director of the industry-affiliation R&D program on Optical I/O at imec. "These exciting nano-ridge laser results represent a significant milestone in using direct epitaxial growth for monolithic III–V integration," he adds. "This project is part of a larger pathfinding mission at imec to advance III–V integration processes towards higher technological readiness, from flip-chip and transfer-printing hybrid techniques in the near term, over heterogeneous wafer- and die-bonding technologies and eventually direct epitaxial growth in the longer term."

www.nature.com/articles/s41586-024-08364-2
www.imec-int.com

Quintessent and IQE establish commercial quantum dot laser & SOA epiwafer supply chain for AI optical interconnects

Quintessent Inc of Santa Barbara, CA, USA — which specializes in heterogeneous integration of quantum dot lasers and silicon photonic integrated circuits (PICs) — and epiwafer and substrate maker IQE plc of Cardiff, Wales, UK have partnered to establish what is said to be the world's first large-scale quantum dot laser and semiconductor optical amplifier (SOA) epitaxial wafer supply chain. Supported by an initial purchase order of $0.5m from Quintessent, the collaboration will see IQE deliver production quantities of epiwafers to Quintessent through 2025.

The ever-growing demand for larger parameter models for AI training and inferencing necessitates the interconnectedness of disaggregated compute and memory resources with high bandwidth, low latency, low energy consumption and high reliability, which can only be met with advanced optical interconnects, say the firms. The laser source within the optical interconnect is a major driver of all these performance metrics, but conventional laser technology and the associated III–V supply chain falls short of AI's future demands.

Reliability of the laser is especially crucial and is perceived to be a limiting factor in scaling optical interconnects for future AI 'factories'. The use of quantum dot material provides a foundational breakthrough for laser and SOA technology, resulting in longer lifetimes for enhanced reliability, wider operating temperatures, higher wall-plug efficiency, lower noise, and higher immunity to back reflections, the firms add.

The supply of high-quality and high-volume quantum dot epitaxial wafers for laser sources and SOAs have been limited until recent breakthroughs were achieved by Quintessent and IQE, which have been in the making for the past decade, including research that was spun out of John Bower's laboratory at the University of California, Santa Barbara. Transitioning the gallium arsenide (GaAs)-based quantum dot research to high-volume production has resulted in highly optimized and high-performing gain material on 6-inch diameter epiwafers that can produce several hundreds of millions of edge-emitting lasers and SOAs per year.

"The performance, cost and reliability advantages that quantum dot-based lasers and amplifiers enable over their quantum well counterparts are exactly what our customers are demanding to address the soaring need for optical connectivity in AI-driven compute," says Quintessent's CEO & co-founder Alan Liu. "Through our partnership with IQE, we have brought this transformative technology to scale, positioning us to be the leader in delivering solutions leveraging quantum dot laser and SOA technology," he adds.

"Our long-term partnership on commercial products and DoD [Department of Defense] programs has yielded QDL [quantum dot laser] wafers with excellent reproducibility and lasing performance," says IQE's chief revenue officer Mark Furlong. "In addition to expertise in volume manufacturing of epitaxial wafers, our partnership with Quintessent demonstrates IQE's strong track record in scaling the manufacturing readiness of new product into volume production."

www.iqep.com
www.quintessent.com

Photon Design previews new quantum dot simulation tool

At SPIE Photonics West 2025 in San Francisco (25–30 January), photonic simulation CAD software developer Photon Design Ltd of Oxford, UK previewed results from its upcoming quantum dot module being added to its established laser simulator HAROLD. The expansion to HAROLD will allow simulation of gain and absorption spectra from epitaxy structures with multiple quantum dot layers using an eight-band k.p model and a full 3D stress-strain model. The module was developed and validated in collaboration with Cardiff University, which has expertise in compound semiconductor photonics.

"HAROLD is a design tool for modelling the epitaxy layer composition of Fabry–Perot and VCSEL [vertical-cavity surface-emitting laser] quantum well lasers," says CEO & founder Dr Dominic Gallagher. "The new HAROLD quantum dot module enables rapid, virtual prototyping and performance verification of the absorption and gain spectra of the quantum dot layers, down to the sizes and distribution of the dots in the epitaxy. This will help inform and improve the supplier's manufacturing process, linking real test results with the simulation model," he adds. "Photon Design provides consistent, technical support for tools like the HAROLD, including involvement with the developers themselves."

HAROLD and the quantum dot module sit within Photon Design's comprehensive CAD environment. This is a library of simulation tools for designing passive components (such as ring resonators, surface grating couplers and arrayed waveguide gratings) up to entire active photonic integrated circuits."

www.spie.org/conferences-and-exhibitions/photonics-west
www.photond.com

PHOTON IP raises €4.75m seed funding led by Innovation Industries, joined by Faber, BOM & PhotonDelta

Funds to accelerate industrialization and commercialization of technology combining silicon photonics with III–Vs

Low-power optical chip maker PHOTON IP of Eindhoven, The Netherlands has raised a €4.75m in a seed funding round, led by Innovation Industries with participation from Faber and Brabantse Ontwikkelings Maatschappij (BOM) and with funding support from Eindhoven-based photonic chip industry accelerator PhotonDelta. PHOTON IP hence aims to accelerate the industrialization and commercialization of its technology, which is said to efficiently combine silicon photonics with active III-V materials.

As optical communication networks, data centers for AI and sensing applications are critically dependent on optical chips. However, the core technologies available to efficiently integrate multiple materials on a single photonic chip are becoming a fundamental barrier, says the firm. Existing schemes for photonic integration can't keep pace with delivering the performance, energy efficiency, and small footprint required. PHOTON IP's technology aims to address this by reinventing the way silicon and various III–V materials such as indium phosphide (for lasers and high-performance modulators) are integrated onto a single photonic chip. The method is said to radically simplify the manufacturing process and open up a path towards mass deployment for advanced low-power optical engines for a wide range of applications.

"We're not just advancing integrated photonics — we're simplifying the manufacturing process for photonic circuits as well," says co-founder & CEO Rui Santos. "With our advanced optical engines, we're setting a new performance benchmark and eliminating the barriers to efficiently combining III–V materials with silicon. This funding expands our ability to grow our team and bring our first products to market," he adds.

"By effectively coupling diverse photonic platforms in a mass-manufacturable process, the company aims to deliver high-performing photonic solutions at volume," says Vincent Kamphorst, investment director at Innovation Industries. "We look forward to supporting PHOTON IP as they develop."

The latest fundraising follows the initial investment by Vigo Ventures in 2021 and the first contracts won with customers worldwide, for which the first products are being co-developed and tested. PHOTON IP says that, since being founded in 2020, its pan-European team has received recognition for its innovation, including grant support of more than €2m from the European Innovation Council.

www.photonip.tech
www.photondelta.com

Malaysia's Globetronics to make POET's optical engines

US$25m public offering to complete after acquisition of China joint venture Super Photonics

POET Technologies Inc of Toronto, Ontario, Canada — designer and developer of the POET Optical Interposer, photonic integrated circuits (PICs) and light sources for the data-center, telecom and artificial intelligence (AI) markets — has signed a master agreement, an optical engine purchase agreement and a deed of consignment with Kuala Lumpur-based Globetronics Manufacturing Sdn Bhd (GMSB) to make optical engines for POET in Penang, Malaysia.

POET has engaged GMSB to assemble and test optical engines based on designs made exclusively by POET. The deed of consignment relates to a suite of wafer-level process equipment recently purchased by POET that is being installed at the GMSB facility in Penang. Concurrent with the deed and a purchase agreement, the parties entered into a master agreement lasting three years that governs the overall relationship between the parties. POET and GMSB have prepared an initial project plan and statement of work for the installation and start-up of the consigned tools, the costs for which will be absorbed by POET. POET will submit purchase orders under the optical engine purchase agreement, with pricing to be based on specific optical engine types. GMSB's parent firm Globetronics Technology Berhad (GTB) has allocated RM7.7m (about US$1.7m) for additional capital expenditures in connection with manufacturing optical engines for POET over the 2025–2027 period.

Separately, and further to the announcement on 25 November of a binding memorandum of understanding (MOU) with Quanzhou Sanan Optical Communication Technology Co Ltd (SAIC) to transfer to POET its 24.8% stake in the China-based joint venture Super Photonics Xiamen (SPX), along with all the production equipment previously leased by SAIC to SPX, POET confirms that the parties expect to soon conclude their ongoing negotiations. Binding definitive agreements are expected to be signed by 31 December. Terms of the transaction with SAIC remain subject to finalization and are expected to be announced upon signing of the definitive agreements POET intends, following completion of the transaction, to continue to operate SPX in a manner consistent with past practice while it brings up a wafer-level assembly operation for optical engines in GMSB, implementing its 'China Plus One' strategy.

Also, POET confirms that its US$25m non-brokered public offering of 5,000,000 units of the corporation at a price of US$5 (C$7.08) per unit (announced on 12 December) has been fully subscribed by a single institutional investor, raising gross proceeds of US$25m. POET anticipates using the net proceeds for working capital and general corporate purposes.

Subject to the receipt of all regulatory approvals (including final acceptance by the TSX Venture Exchange) and the satisfaction of other customary conditions, closing of the offering is now expected after completing the SPX acquisition.

www.poet-technologies.com

US CHIPS Incentives Program awards finalized for Corning, Edwards Vacuum and Infinera

Amended award for GlobalFoundries to support advanced packaging of photonic integrated circuits

Under the CHIPS Incentives Program's Funding Opportunity for Commercial Fabrication Facilities, the US Department of Commerce has finalized three separate awards of direct funding, comprising: up to $32m for Corning, up to $18m for Edwards Vacuum, and up to $93m for Infinera.
The awards come after the previously signed preliminary memoranda of terms, announced on 8 November, 10 October and 17 October 2024, respectively, and the completion of the Department's due diligence. The Department will disburse the funds based on the companies' completion of project milestones.

The awards support the following projects:

- **Corning** (Canton, New York): Up to $32m will enable Corning, one of the largest industrial employers in New York's North Country region, to increase production of Corning HPFS (high-purity fused silica) and EXTREME ULE Glass (Ultra Low Expansion Glass) and scale a novel technology manufacturing process in Canton. HFPS and ULE materials are key components of deep ultraviolet (DUV) and extreme ultraviolet (EUV) lithography machines and photomasks, and this new technology would improve EUV performance with a lower carbon footprint. The investment in Corning will enable a reliable domestic supply of these important components in the USA and is expected to help to advance US technology leadership in the lithography supply chain. The project should create about 130 manufacturing jobs and over 175 construction jobs. Corning's project will also be supported by a commitment of up to $7m by Empire State Development in performance-based Excelsior Jobs Program funding to support the building of computer chips.
- **Edwards Vacuum** (Genessee County, New York): Up to $18m will support the construction of a greenfield manufacturing facility in Genesee County, New York and will produce dry vacuum pumps, creating up to 100 construction jobs and 500 production jobs. The investment will help to create a reliable domestic supply of important equipment for semiconductor manufacturing and is a step towards strengthening US economic and national security, as there is currently no domestic production of semiconductor-grade dry vacuum pumps, which are essential for both advanced and legacy semiconductor fabrication.
- **Infinera** (San Jose, California; Bethlehem, Pennsylvania): Up to $93m will support the construction of a new fab in San Jose, California, and a new advanced test & packaging facility in Bethlehem, Pennsylvania, which should increase Infinera's existing domestic manufacturing capacity by an estimated factor of 10. Infinera is a vertically integrated photonic semiconductor and telecoms equipment manufacturer that has operated its US fabrication and advanced test & packaging facilities for over 20 years. As the USA becomes more reliant on larger amounts of data driving increased energy usage, Infinera's indium phosphide-based photonic integrated circuits (InP PICs) are increasingly important. The PICs and optical modules are key components in optical network communications and enable the fast, reliable transfer of large amounts of data communications, spanning short- to long-distance broadband networks connecting cities, countries and continents; between data centers; and between artificial intelligence (AI) and machine learning (ML) clusters inside the data center. This investment will create about 500 manufacturing jobs and 1200 construction jobs.

"We have finalized the agreement to receive CHIPS Act funding to increase photonic semiconductor fabrication and packaging in the US and help protect our national security by enabling us to better compete with foreign adversary nations," says Infinera's CEO David Heard. "This funding will accelerate delivery of US photonic semiconductor innovations to meet the demands of critical network infrastructure in the era of AI," he adds.

In addition, the Department of Commerce has amended the previously announced award to provide a supplemental award of up to $75m in direct funding to GlobalFoundries, to support the expansion of its existing facility in Malta, New York, to provide first-of-its-kind advanced packaging technology and enable for a fully integrated pure-play foundry wafer manufacturing and advanced packaging process flow in the USA. The firm's expanded capabilities will focus on the packaging of photonic integrated circuits, which will enable faster networking and communications to support AI and high-performance compute end-markets, in addition to chiplet integration and wafer-to-wafer hybrid bonding. Through the company's partnership with the US Department of Defense, the investment will establish domestic capability for an end-to-end trusted process flow to meet US national security needs.

www.infinera.com
www.chips.gov
www.nist.gov/chips

First Solar endows Missouri S&T professorship in Critical Energy Materials

Investing in workforce education to help secure supply chains

Cadmium telluride (CdTe) thin-film photovoltaic (PV) module maker First Solar Inc of Tempe, AZ, USA has established the Endowed Professorship in Critical Energy Materials in the materials science and engineering department at Missouri University of Science and Technology (Missouri S&T).

The decision reflects the strategic alignment between the two organizations, which have collaborated on critical minerals, particularly tellurium, for the past decade.

"We recognize Missouri S&T's unparalleled depth of expertise in responsible production of critical energy materials," says First Solar's chief supply chain officer Mike Koralewski.

Dr Michael Moats, professor and chair of materials science and engineering at S&T, has worked with First Solar for many years, advising it on existing tellurium supply and opportunities to increase affordable and sustainable recovery of the metalloid from existing operations. He believes that First Solar's endowment is key to Missouri S&T's strategy to be a leader in critical minerals research by developing expertise on important points across the supply chain that governs each mineral's journey to the marketplace.

"The position will plug into our team and complement the expertise we already have throughout the supply chain, from policy and economics to cleaning up afterwards," says Moats.

Missouri S&T is home to the Thomas J. O'Keefe Center for Critical Minerals, which supports research and other scholarly activities, including the fourth annual Resilient Supply of Critical Minerals workshop funded by the US National Science Foundation, which S&T hosted in August.

In addition, Missouri S&T leads the Critical Minerals and Materials for Advanced Energy Tech Hub consortium, which in October 2023 was selected as one of 31 tech hubs; the Tech Hub Program is administered by the US Department of Commerce's Economic Development Administration.

"Other economies dominate the global market for certain elements and, when restrictions are placed on those elements, there's the potential to disrupt manufacturing, slow down our fight against climate change and impact our national security," Moats says. "By ensuring that extractive metallurgy is taught at a college level, First Solar is helping us address these challenges."

First Solar says that it is committed to investing in the education of the next-generation workforce that will enable the mining industry to better support the green energy transition. By endowing the professorship, it aims to foster research and education that will equip future professionals with the skills and knowledge needed to advance the mining and materials industries. The investment is reckoned to be crucial for developing innovative solutions and technologies that will drive the green energy transition and ensure a sustainable future.

Koralewski says that First Solar's hope is to support research that benefits as many people and organizations as possible.

"As America's solar company, we want to help enhance our country's critical mineral security by enabling Missouri S&T," he says. "If discoveries made as part of our collaboration with Missouri S&T can be disseminated and more widely adopted, it will have a much more meaningful impact."

https://criticalminerals.mst.edu/
www.firstsolar.com

CSA Catapult outlines steps to create UK semiconductor 'super cluster' and drive long term growth and exports

Recommendations include a National Semiconductor Institute, a Semiconductor Challenge Fund, prioritizing UK semiconductors in public contracts, and skills plans.

The UK semiconductor industry is at a critical stage in its evolution, according to Martin McHugh, CEO at Compound Semiconductor Applications (CSA) Catapult (a not-for-profit center of excellence established in 2018 by government agency Innovate UK that specializes in the measurement, characterization, integration and validation of compound semiconductor technology spanning power electronics, advanced packaging, radio frequency and microwave, and photonics applications).
As Europe, the USA, China, Japan and South Korea invest, there is a significant risk of the UK being left behind, he adds.

In early November, the European Union (EU) invested €170m in 27 Chips Competence Centers to improve technical expertise and boost skills. In the USA, the government is fast-tracking $39bn-worth of subsidies to support its semiconductor industry. The UK cannot compete financially with these countries, notes McHugh.

"The UK industrial strategy provides an opportunity to capitalize on our strengths and chart a new course for the industry. These strengths include chip design, R&D, IP and compound semiconductors," McHugh says. "Semiconductors are essential to delivering the industrial strategy. They are everywhere in modern life and underpin several key industries, including automotive, defence, aerospace, health, telecoms and manufacturing."

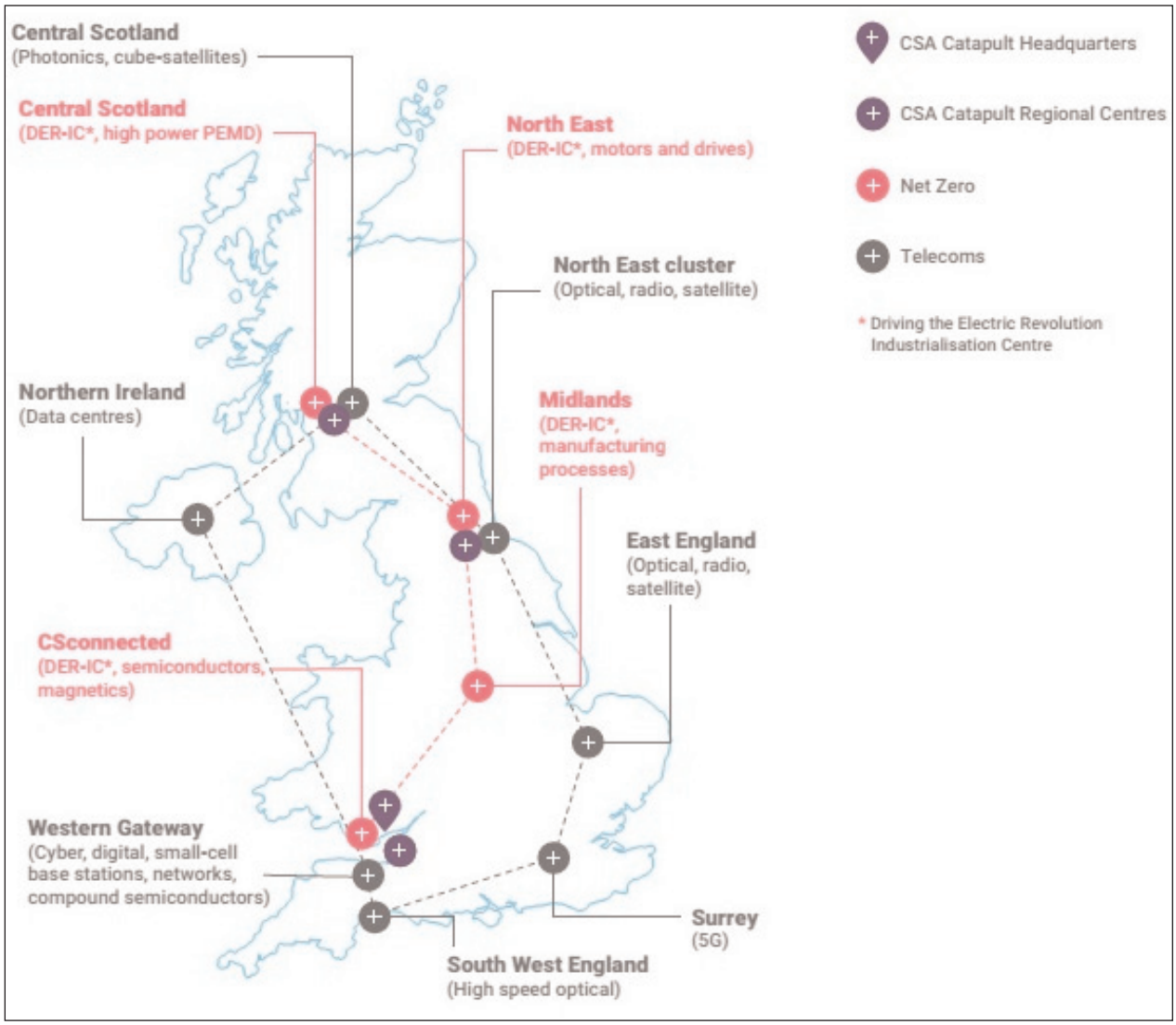
In response to the UK government's new industrial strategy, CSA Catapult has published eight recommendations to address industry challenges and to support existing areas of strength and deliver growth:
1. elevate the importance of the semiconductor sector by recognising semiconductors as a subsector of the industrial strategy;
2. create a National Semiconductor Institute to strengthen, lead and co-ordinate targeted activity across the UK;
3. coordinate long-term skills plans for semiconductors across UK and devolved governments to maintain and grow talent pools;
4. position the UK as a 'semiconductor super cluster' to drive UK growth and exports for the long term by establishing a £305m Semiconductor Challenge Fund;
5. grow existing semiconductor clusters to develop regional capability and support regional growth;
6. invest in compound semiconductor manufacturing and infrastructure;
7. prioritize UK semiconductors in public contracts for digital infrastructure and defence;
8. increase access to funding, improve regulation and strengthen IP.

Making semiconductors a national priority

Specifically, CSA Catapult recommends that semiconductors are recognized as a subsector of the industrial strategy. "Semiconductors underpin the UK's economy, national security and everyday technology. Without them, we would not have smartphones, electric cars, solar panels, satellites, medical scanners and much more," notes McHugh. "Semiconductors are being used to build green technologies and help tackle climate change. The industry must be given the attention and investment it deserves."

Strengthen and co-ordinate activity

There are over 200 dedicated semiconductor companies in the UK, which collectively generate £9.6bn in revenues and employ 15,000 people. Clusters of expertise are in South Wales, the South West, Cambridge, the North East, Northern Ireland, and Scotland. However, the industry lacks a single, independent, unified voice to bring these clusters together, promote the sector and attract international investment. "That is why we're calling for the creation of a National Semiconductor Institute to strengthen, lead and co-ordinate targeted



activity across the UK," says McHugh. "A key role of the Institute will be to grow existing semiconductor clusters in the UK and unleash the full potential of our cities and regions."

Investing in infrastructure to build a UK semiconductor super cluster

"To grow our clusters, we need investment," notes McHugh. CSA Catapult has laid out a £305m Semiconductor Challenge Fund to provide UK clusters with critical infrastructure. This would include a £150m investment in regional projects such as a UK Centre of Excellence for quantum photonic integrated circuits (PICs) and a world-first center for AI-powered electronics, photonics, quantum and design automation (AI.EPQDA).

The recommendations also include investment in compound semiconductor manufacturing and infrastructure, specifically open-access fabrication plants specializing in silicon carbide (SiC), gallium nitride (GaN) and gallium arsenide (GaAs) to remove commercialization and scale-up barriers for start-ups and SMEs and to allow them to grow quickly and efficiently.

Creating a talent pipeline

"The UK's semiconductor sector can only grow if we have the right people with the right skills driving it forward. There is currently a shortage of skilled engineers with the knowledge and experience to work on the next generation of semiconductor technologies," notes McHugh. "The role of a National Semiconductor Institute will be to coordinate policy development across the UK and close this skills gap," he adds. "We also recommend the UK and devolved governments invest in long-terms skills plans to create programs and pathways that attract a greater and more diverse talent pool into the industry."

Removing barriers

"To grow the UK semiconductor industry, we must also provide opportunities for the sector to support national interests, such as prioritizing UK companies for defence and digital infrastructure contracts," says McHugh. "We must also remove barriers by increasing access to funding, improving regulation and strengthening IP. It is encouraging to see the government make progress on the National Wealth Fund and unlocking UK pension funds to increase access to both public and private funds.

"The UK semiconductor industry has enormous potential. It is growing fast and is estimated to be worth £13–17bn by 2030. Our recommendations will build on existing strengths, support regional clusters and drive growth in this critical sector across the UK," McHugh concludes. ■

https://csa.catapult.org.uk/wp-content/uploads/2024/11/catapult-POLICY-PAPER_FINAL.pdf

Indium phosphide laser on silicon nitride photonic circuit

Micro-transfer printing integration achieves wavelength tuning over 54nm in the C and L bands.

Researchers based in Belgium and France have used micro-transfer printing (MTP) to integrate indium phosphide (InP) laser gain material on a silicon nitride (Si_3N_4) photonics platform [Biwei Pan et al, Photonics Research, v12, p2508, 2024].

The team from Ghent University–IMEC in Belgium, Thales Research and Technology in France, I MEC in Belgium and III–V Lab in France reports: "The gain section consists of an aSi:H [amorphous hydrogenated silicon] rib waveguide with an InP coupon micro-transfer-printed on top. A 4µmx840µm gain mesa together with 180µm-long tapers at each side is used to provide sufficient gain for lasing and realize optical coupling between the coupon and aSi:H waveguide."

Such devices are needed for high-capacity long-haul coherent communication systems, sensors, and microwave photonics. The researchers also see the large tuning range as benefiting large-steering-angle optical phase array (OPA) and high-axial-resolution optical coherence tomography (OCT) systems.

The attractions of the Si3N4 photonics platform over competitors such as silicon-on-insulator (SOI) include much lower propagation losses and much higher on-chip power handling for optical communications. However, the platform is difficult to combine with InP since the optical coupling between the materials is hampered by a large refractive index mismatch. The research team has previously overcome this by using an intermediate hydrogenated amorphous silicon (aSi:H) bridge between the Si_3N_4 and InP optical fields.

The Si_3N_4 platform (Figure 1) allowed the researchers to design a tunable laser with an overall chip size of just 5.6mmx0.8mm — "much more compact compared to the laser cavity on the shallow etched silicon waveguide," according to the team.

A disadvantage of the Si_3N_4 platform is a poor thermo-optic coefficient ($2.45x10^{-5}$/K), making the usual thermal wavelength tuning of the Si_3N_4 waveguides more difficult, compared with silicon, requiring extensive simulation and design studies.

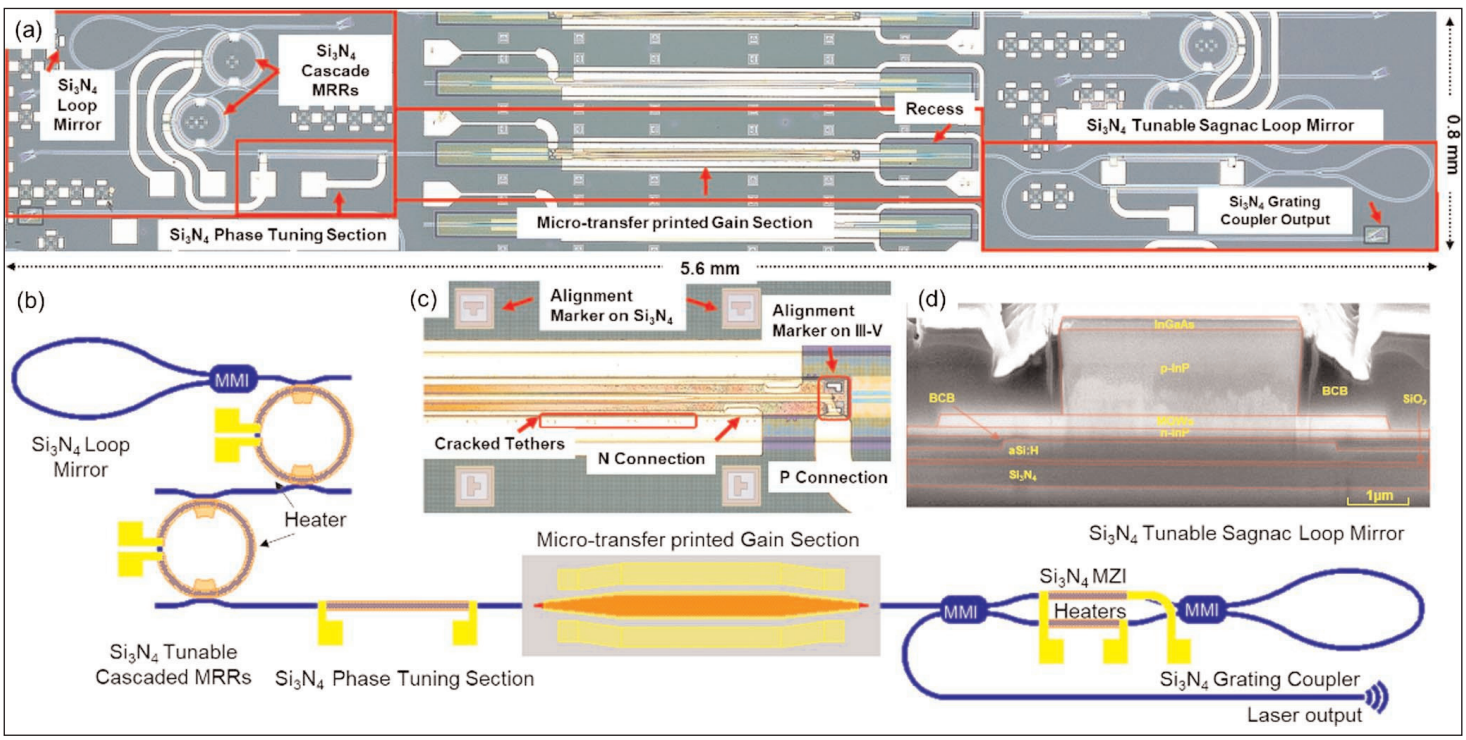


Figure 1. (a) Microscope picture of tunable laser. (b) Corresponding schematic diagram of cavity structure (MRR, micro-ring resonator; MMI, multimode interferometer). (c) Zoom-in view of MTP III–V gain section on aSi:H/Si_3N_4 waveguides. (d) Scanning electron microscope (SEM) cross-section image.

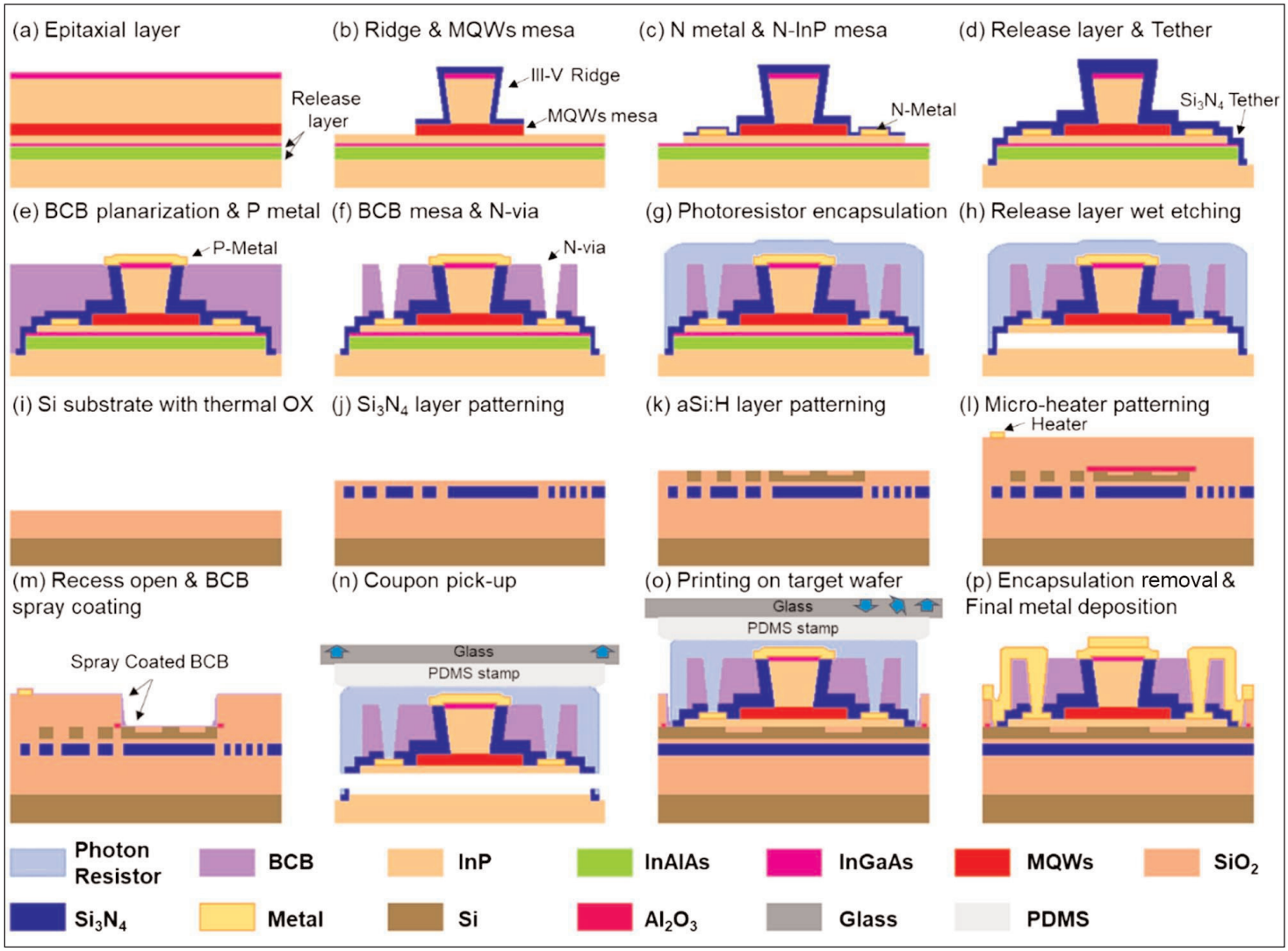


Figure 2. Schematic process flow of (a)–(h) active coupons on III–V-substrate for micro-transfer printing, and (i)–(m) Si_3N_4/aSi:H circuits and preparation on the target substrate, and (n)–(p) heterogeneous integration and post-processing.

The III–V Lab facility manufactured the InP optical gain structures (Figure 2). The release layers consisted of 50nm indium gallium arsenide (InGaAs) and 150nm indium aluminium arsenide (InAlAs), allowing selective etch against InP.

The fabrication constructed the ridge waveguide and multiple quantum well (MQW) mesa structures. The n-metals were then deposited, followed by pattern and etch down to the release layers. Silicon nitride covered the gain structure and provided tethering of the assembly after the release layers were removed.

The regions between the devices on the wafer was filled with divinylsiloxane–bis-benzocyclobutene (DVS–BCB), and planarized to expose the p-contact region. The p-side metal was applied, and vias to the n-metal contacts made. The DVS–BCB material was also etched to give access to the release layers.

The coupons were then encapsulated with photoresist, and the release layers under-etched using an iron trichloride ($FeCl_3$) water solution, keeping Si_3N_4 tethers holding the coupon in place.

The researchers comment: "All the III–V-based processes are done on the source wafer, which indicates that different III–V devices can be integrated on the Si/SSi_3N_4-based photonic circuits simultaneously without increasing the process complexity. This advantage is crucial for the Si_3N_4 platform since it is purely passive and requires all the active building blocks."

The passive Si_3N_4 photonic circuits were manufactured at IMEC's 200mm pilot line. The silicon substrate incorporated a 2.5µm thermal oxide top layer. A 400nm Si_3N_4 layer was chemical vapor deposited (CVD) at low pressure on top of 700nm high-temperature plasma-enhanced CVD (PECVD) silicon dioxide (SiO_2). The Si_3N_4 photonic circuit was patterned with deep ultraviolet (DUV) photolithography, followed by plasma etch.

A further high-temperature PECVD SiO_2 layer covered the photonic structures, followed by planarization to 100nm above the Si_3N_4 waveguides.

The 330nm amorphous hydrogenated silicon (aSi:H)

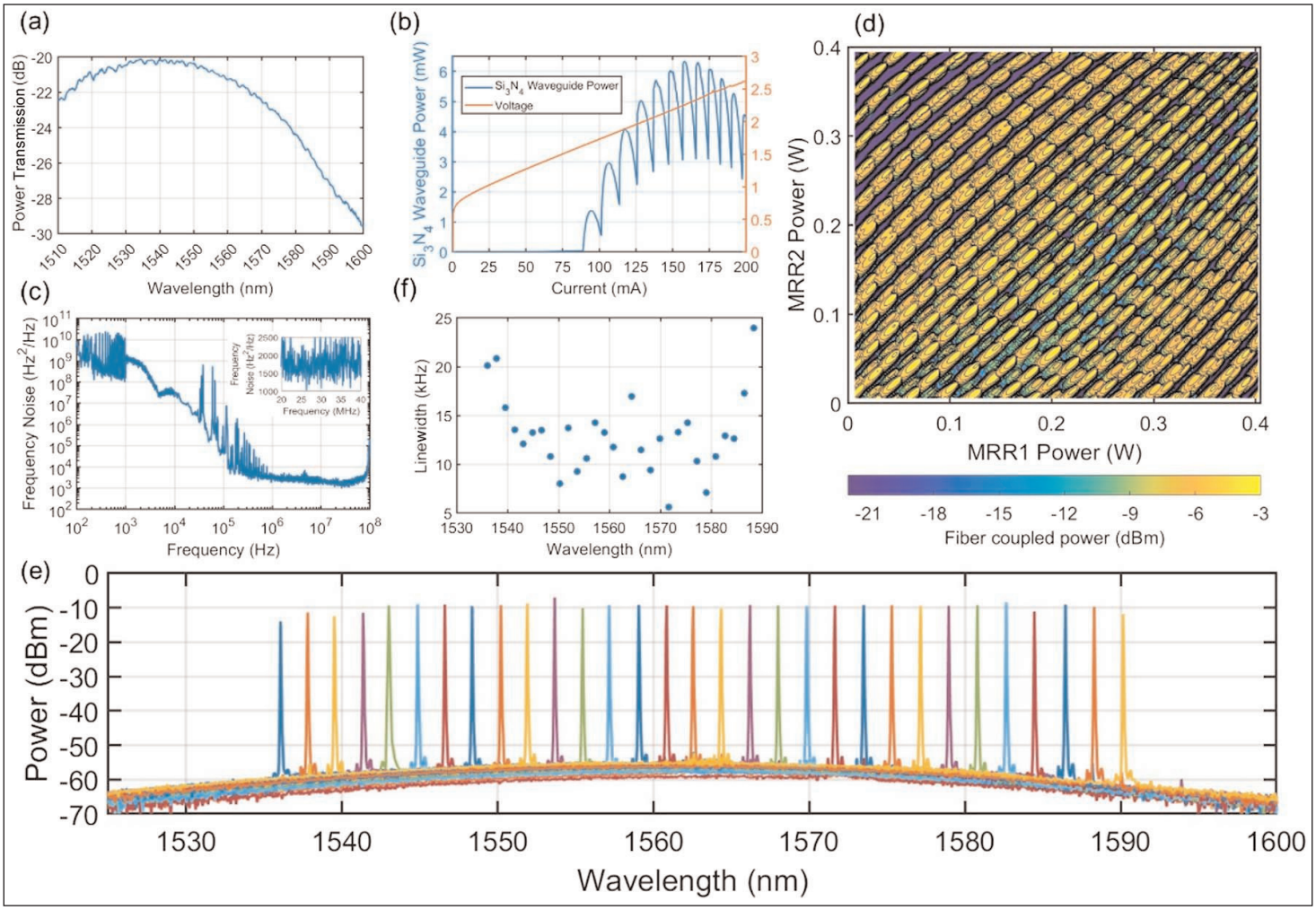


Figure 3. (a) Transmission spectrum of reference waveguide with grating couplers at both sides. (b) Laser light output–current–voltage (LIV) behavior. (c) Frequency noise spectrum at 1571.56nm (inset: zoom-in from 20MHz to 40MHz). (d) Two-dimensional output power tuning map. (e) Optical spectra under different operation wavelengths. (f) Lorentzian linewidths versus wavelength.

was also deposited by PECVD, along with a 100nm PECVD Si_3N_4hard mask. Rib and strip waveguides were patterned in the aSi:H. The wafer was covered with PECVD SiO_2 and planarized. The hard mask material was removed by etch-back.

The photonic wafer was then cleaved into separate samples for further processing. A 50nm aluminium oxide (Al_2O_3) etch-stop layer was electron-beam evaporated and patterned before a 1.5µm PECVD SiO_2 top layer was added. Micro-heaters were created next on top of the photonic structures.

Recesses were made through to the aSi:H structures to enable evanescent coupling. The researchers explain the purpose of the etch-stop material: "The Al_2O_3 is used as the etch-stop layer to maintain the quality of the surface in the recess for the following bonding process."

The Al_2O_3 was removed before a thin 100nm DVS–BCB bonding layer was spray-coated and soft-baked at 150°C. The team comments: "Buildup of the DVS–BCB at the side walls of the recess benefits the following metal connection."

The researchers used a single-post elastomeric poly-dimethylsiloxane (PDMS) stamp to pick up the 1260µmx45µm III–V coupons for MTP to the photonic circuit.

The team comments: "Although a single-post stamp was used in this experiment, printing of multiple devices at the same time can be realized by using a dedicated stamp with multiple posts."

Alignment of the coupons to the target position was made through digital pattern recognition markers on both material structures.

The bond was made after removal of the photoresist encapsulation through curing the DVS–BCB at 280°C. The material was found to shrink some 80nm during the curing process. The final wiring was achieved by depositing and patterning a thick layer of titanium/gold (Ti/Au) after removal of DVS–BCB residues.

The team comments: "During printing and post-printing processing, there are neither processes for source and target materials, nor processes requiring high temperature, which means the source and target wafers can be fully implemented in their own established

foundries, which greatly facilitates mass production and time to market."

The fabricated laser achieved a 87.6mA threshold with the laser output power reaching 8.3mW at 158.5mA injection (Figure 3). The operating wavelength was 1571.56nm. The temperature was maintained at 15°C using a thermo-electric cooler.

The researchers comment: "As the gain section sits on a thick buried oxide layer, thermal roll over starts at an electrical power dissipation of around 346mW. The output power could be further improved by reducing the series resistance and the thermal resistance."

The intrinsic linewidth was 5.6kHz, according to white-noise-limited frequency measurements. "This linewidth can be influenced by the deviations of the MRR's self-power coupling ratio, as well as waveguide loss and coupling loss in the experiments," the team explains.

The wavelength-tuning effects of the MRR heaters was mapped out at 158.5mA. The researchers comment: "The variation in the output power originates from how well the spectra of the MRRs and the cavity modes are aligned to each other at the setpoints. The local peaks in the tuning map occur at precise alignment, which were extracted as the working points of the laser. The laser can be locked to such bias points through a feedback loop to get the preferred working conditions."

The tuning range was 54nm with more than 40dB side-mode suppression ratio (SMSR). The linewidth was less than 25kHz across this range. The wavelengths fall in the conventional/C (1530–1565nm) and long/L (1565–1625nm) fiber-optic bands. The free spectral range (FSR) was extended beyond the usual Vernier value for two MRRs of about 25nm to three periods. Further extension is presently blocked due to gain bandwidth limitations.

The Sagnac loop enabled reflectivity adjustment of the laser output by applied power input to the micro-heaters changing the optical phase difference between the Mach–Zender interferometer (MZI) sections. ■

https://doi.org/10.1364/PRJ.530925

Author: Mike Cooke

Graded barriers bandwidth boost for micro-LEDs on silicon

Devices achieve a −3dB bandwidth (f_{-3dB}) of 580MHz at 2000A/cm^2.

South China University of Technology and Guangdong Choicore Optoelectronics Company Ltd report on using graded indium gallium nitride (InGaN) quantum barriers (QBs) in blue light-emitting diode (LED) to improve the modulation frequency performance of devices grown on silicon (Si) with a view to deployment in visible light communication (VLC) systems [Lei Lei et al, IEEE Electron Device Letters, volume 46 (2025), issue 1 (January), p28].

The team sees VLC as a potential supplement to the overcrowded spectrum of existing wireless communication systems. "However, the lack of LED performance severely limits the development of VLC," the researchers point out.

VLC could be used in systems aimed at short-range positioning data exchange, indoor internet, etc. Such systems can be integrated into existing lighting infrastructure. Normal-size LEDs tend to have relatively

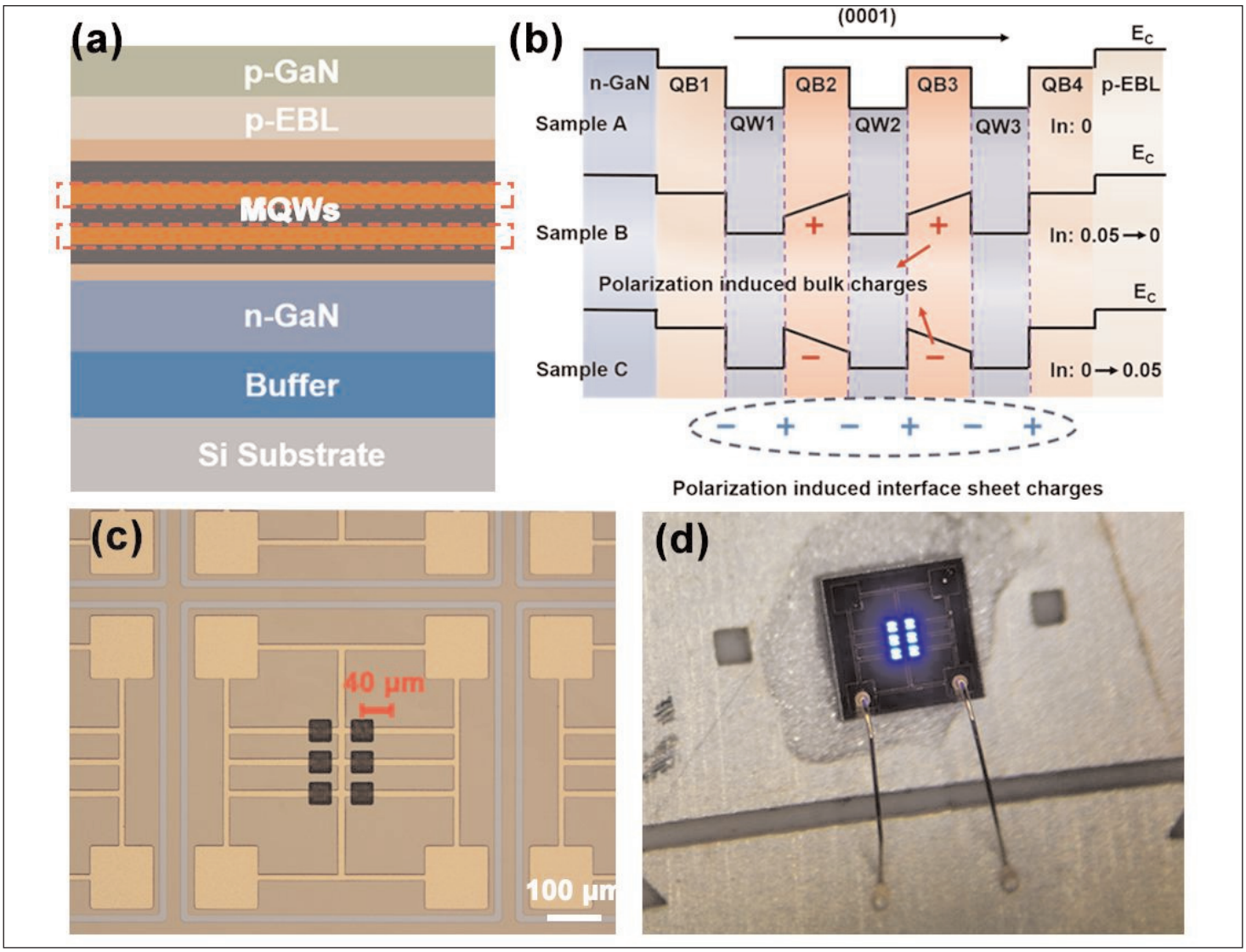


Figure 1. Schematic diagrams: (a) Si-substrate GaN-based LED epitaxial structure, and (b) conduction band for three samples. (c) Optical microscope image of sample, and (d) image of sample C operating at 10A/cm^2.

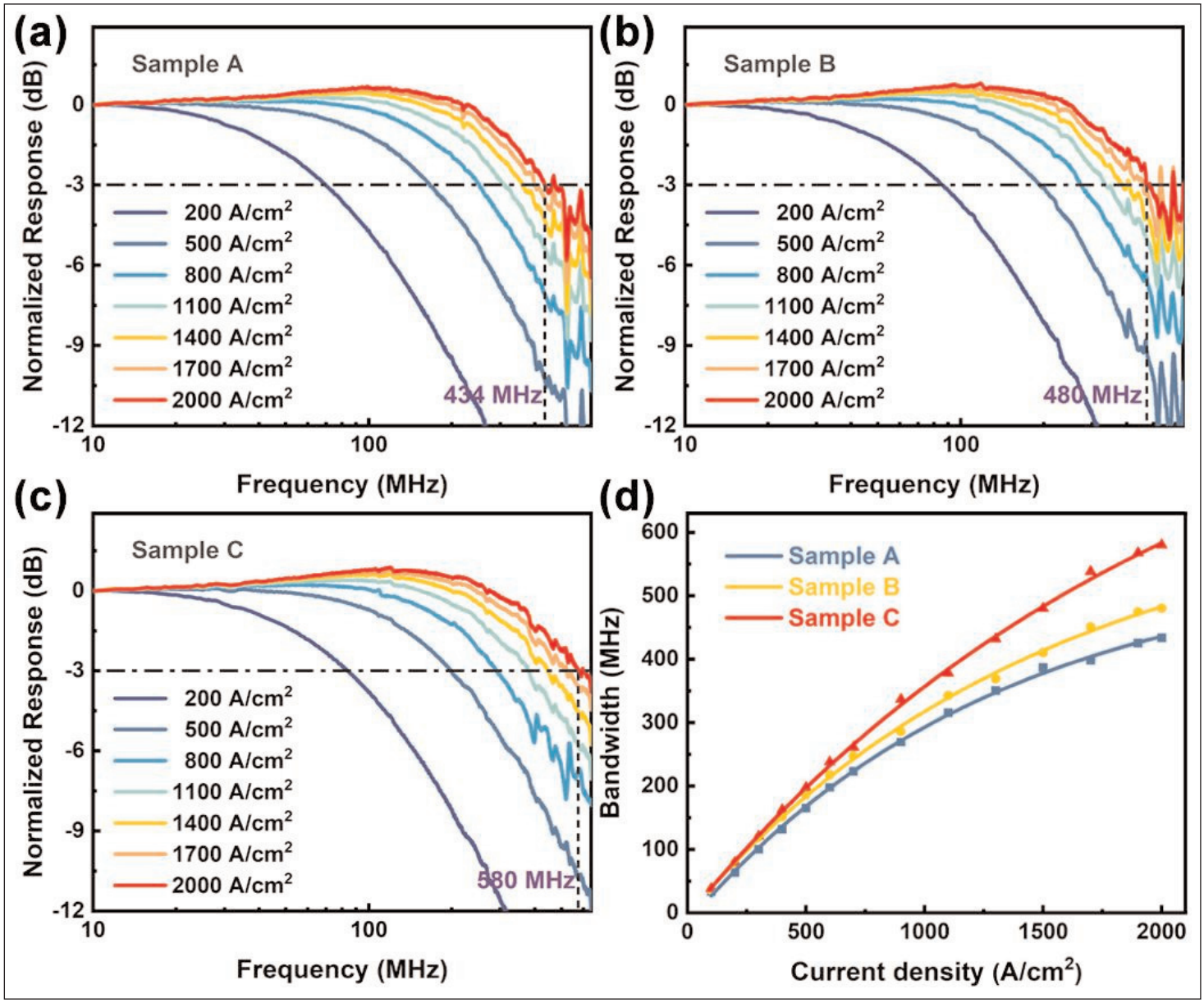


Figure 2. (a)-(c) Frequency responses of samples A–C under different current densities. (d) –3dB bandwidth versus current density.

low modulation bandwidths in the tens of MHz range. This can be improved by reducing the size of the LEDs. One drawback is that the smaller devices have lower light output power (LOP), impacting the signal-to-noise ratio.

One of the blockages to improving the frequency performance of InGaN LEDs is the built-in electric fields that arise from charge polarization contrasts of the III–nitride device layers. These fields tend to reduce the radiative efficiency due to the field pulling apart the electrons and holes that need to combine to emit photons.

By grading the InGaN barriers the researchers hoped to screen these fields, improving both bandwidth and LOP performance.

The epitaxial structures used included 3μm n-GaN contact, 3x(3nm/4nm) $In_{0.16}Ga_{0.84}N/In_xGa_{1-x}N$ multiple quantum well (MQW), 30nm p-type aluminium gallium nitride electron-blocking layer (EBL), and 60nm p-GaN contact layers (Figure 1). Three samples were processed with different $In_xGa_{1-x}N$ profiles in the QBs: sample A had conventional pure GaN in the QBs 1–4 (i.e. x=0); sample B had the middle two QBs, 2 and 3, linearly graded from 5% to 0% along the (0001) growth direction, with the outer barriers pure GaN; and sample C had the QBs graded in the opposite sense, from 0% to 5%.

According to simulations, the effect of the grading in sample C was to elevate the height of the triangular deep potential well between the last QB and the EBL, while diminishing the height of the valence-band barrier.

The team comments: "Such alterations are conducive to enhancing hole injection efficiency and mitigating electron escape, achieving a simultaneous increase in bandwidth and LOP of samples."

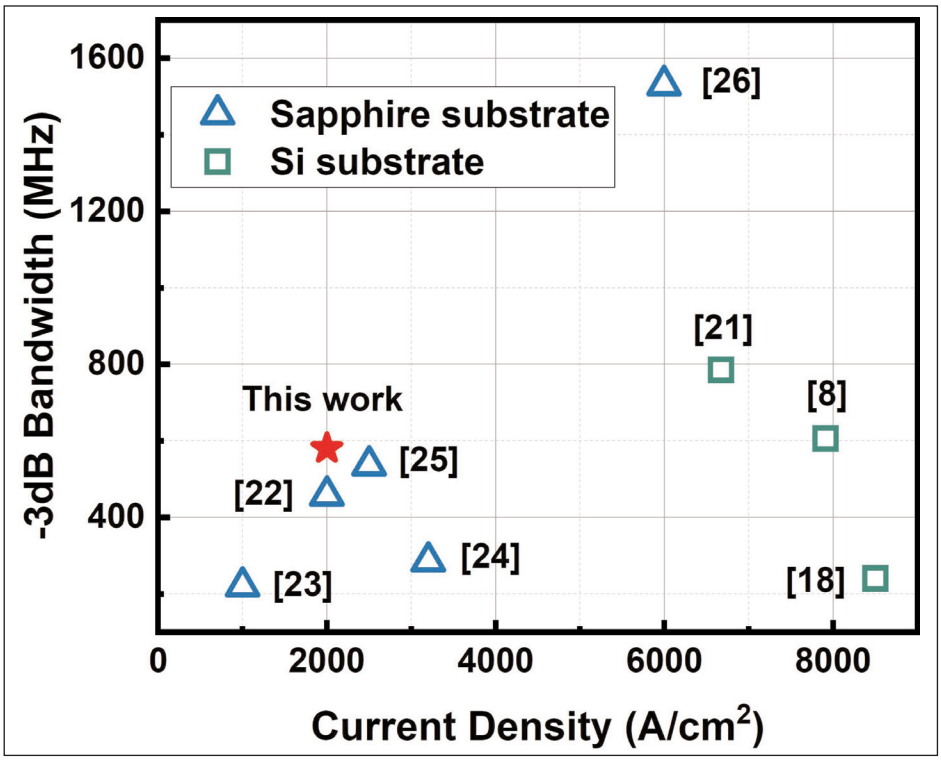


Figure 3. Comparison of −3dB bandwidth for micro-LED arrays with previous reports.

The epitaxial material was fabricated into 2x3 arrays of micro-LEDs flipped onto a silicon conductive circuit substrate and bonded with gold/tin (Au/Sn). The micro-LEDs included a silver (Ag) reflector on the p-contact layer. The individual micro-LED units measured 40μmx40μm. The n-GaN contact layer was wired in parallel with sputtered titanium/aluminium/platinum/gold (Ti/Al/Pt/Au).

The devices needed slightly different forwardvoltage biases to give 1000A/cm^2 current injection: 3.46V for sample A, and 3.44 and 3.41V for B and C, respectively.

The team comments: "Sample A has the highest voltage, potentially because of the higher series resistance and lower crystal quality. Moreover, the weaker polarization field in sample C decreases the height of triangle barrier of the valence band that the carriers need to overcome to inject into the MQWs, and thus the forward voltage."

Sample C also showed 11% improvement over A in terms of light output power (LOP) — 28.9mW, compared with 26.1mW at 2000A/cm^2. Array B had a LOP of 26.7mW at the same current injection point.

The peak wavelength shifted to shorter wavelengths in moving from low to medium current injection: 22nm in sample A, 19.1nm for B, and 17.9nm for C. The peak wavelength at the lowest current was around 450nm (~5nm higher for A, and ~5nm lower for C) The smaller shifts in B and C was attributed to the InGaN grading, and for C the favorable charge polarization configuration in the barriers. The external quantum efficiency for sample C was also improved by 10% over that of sample A (~5%) at 2000A/cm^2.

Sample C also demonstrated a higher −3dB bandwidth — 580MHz at 2000A/cm^2, compared with 434MHz and 480MHz for samples A and B, respectively (Figure 2).

The researchers comment: "The enhancement in −3dB bandwidth could be due to the weaker polarized electric field, which favors accelerated carrier radiative recombination. Concurrently, the lowered triangle barrier of the valence band causes an increase in hole concentration within the active region, thereby further enhancing the radiative recombination coefficient B."

Comparing the bandwidth with previous research shows the South China/Guangdong sample C devices to have performance comparable to those grown on sapphire: high bandwidth at lower injection current density, compared with reports of LEDs on silicon. ■

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Boron enables AlN on silicon growth without cracks

Aluminium nitride layers have been produced with low dislocation density.

Researchers based in Saudi Arabia and Taiwan report on the ability of boron (B) added to aluminium nitride (AlN) to allow the growth of thicker AlN layers on silicon (Si) without cracking [Mingtao Nong et al, Appl. Phys. Lett., v125, p172107, 2024].

The BAlN was used as a buffer layer. The thickness of AlN achieved without cracking was 520nm, the thickest reported, according to a benchmark graph (Figure 1) presented in the paper.

The researchers from King Abdullah University of Science and Technology (KAUST) in Saudi Arabia and National Yunlin University of Science and Technology in Taiwan comment: "Employing TEB [triethyl-boron] flow during buffer layer deposition not only enables achieving a maximum thickness of 520nm without cracking but also results in the lowest full-width at half maximum (FWHM) values for both 002 and 102 planes compared to those in other studies."

The team sees potential for high-electron-mobility transistors (HEMT), high-power devices, piezoelectric sensors, and solar-blind photodetectors. The ultrawide bandgap of AlN (6eV) increases the critical electric field before breakdown, potentially allowing smaller devices to handle larger voltages thus achieving higher-power-density capability.

Although AlN would preferably be grown on native AlN substrates, such material is much more expensive than silicon. Further, an attractive possibility for AlN/Si would be highly integrated AlN devices coupled to mainstream silicon integrated circuitry.

The need for buffer layers between Si and AlN arises from lattice and thermal expansion mismatches of 19% and 43%, respectively. AlN growth is carried out at very high temperature in the range 900–1200°C. When cooled, such material tends to crack as the Si and AlN lattices contract at different rates.

The researchers comment: "The introduction of such a BAlN buffer layer presents two primary advantages: it significantly delays coalescence, thus reducing accumulated stress; and it compensates for the tensile stress caused by the larger lattice parameter of silicon compared to AlN by introducing compressive stress from the smaller lattice parameter of BAlN."

The AlN layers were grown on 2-inch silicon by metal-organic chemical vapor deposition (MOCVD). The precursors were trimethyl-aluminium (TMAl) and ammonia (NH_3). Boron modification was achieved by adding triethyl-boron (TEB) to the inputs.

Three samples were grown. The buffer was grown at 950°C with a V/III ratio of 16,500 for 10 minutes. The samples 1–3 were distinguished by the B/III mole flow ratio: 0%, 20% and 40%, respectively. Sample 1 was thus an AlN reference without B modification.

On top of the buffer the main AlN layer was grown at a high temperature of 1150°C at a 110 V/III ratio. The reactor pressure was maintained at 7.5kPa throughout buffer and AlN growth.

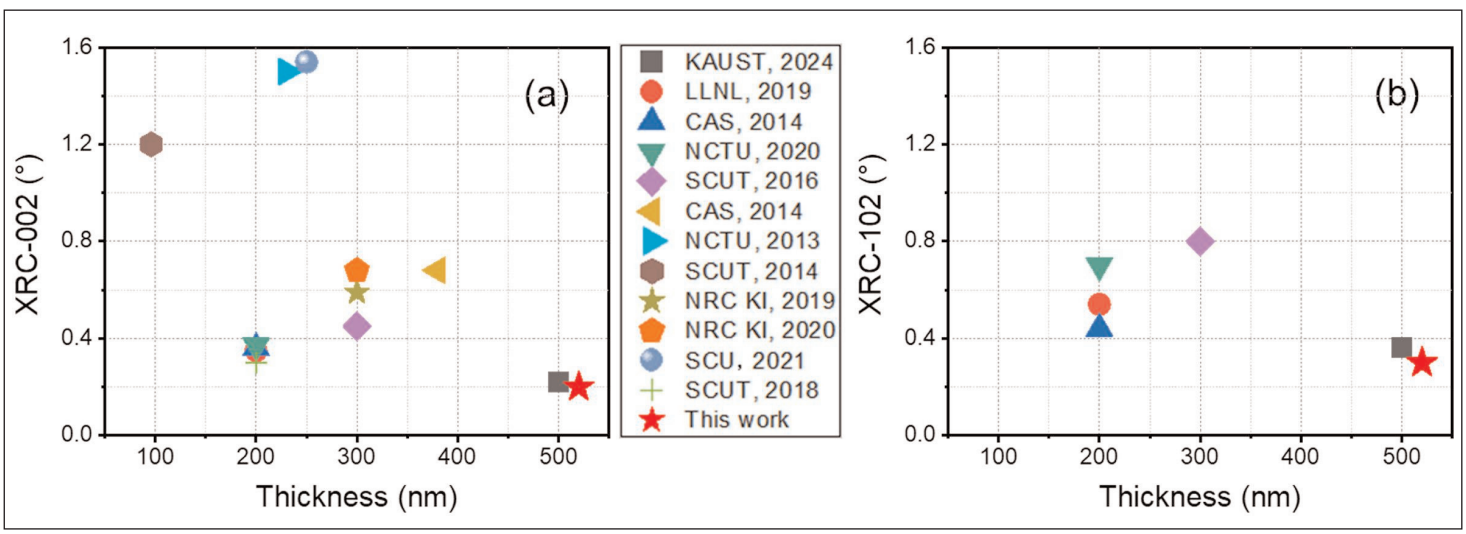

Figure 1. Benchmarks across a range of studies of MOCVD AlN films on Si (111) substrates: thickness versus full-width at half maximum (FWHM) values for x-ray rocking curves (XRC) from (a) (002) and (b) (102) planes.

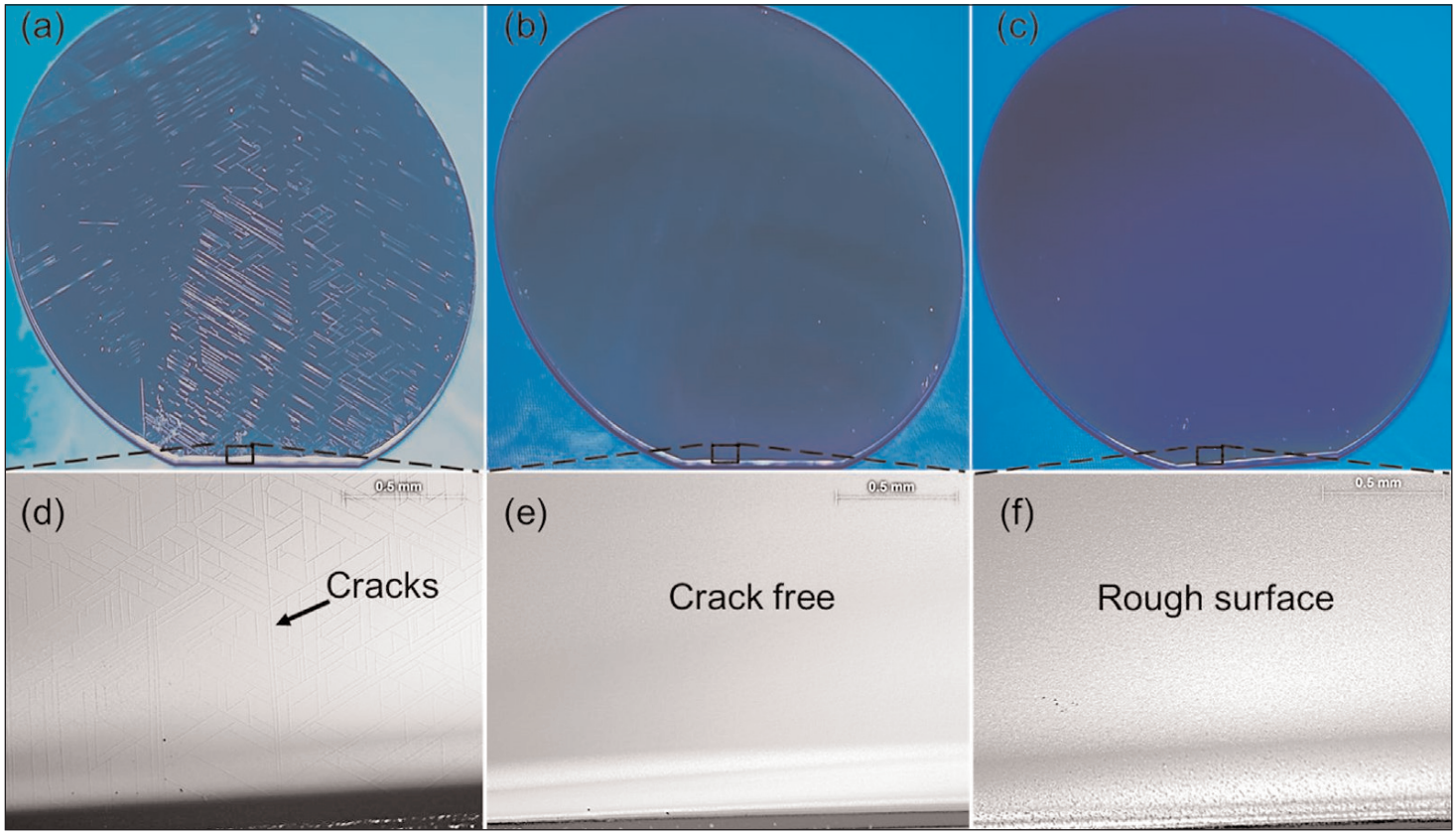

Figure 2. Photographs and optical microscopy images (500x) for samples 1 (a, d), 2 (b, e), and 3 (c, f).

Reflectance measurements made 'in-situ' during the growth showed different coalescence behaviors of the initial islands of III-nitride material: around 200nm and 400nm for samples 1 and 2, respectively. The researchers comment: "This delayed coalescence suggests a reduction in residual stress and defects."

Sample 3 suffered from insufficient coalescence and resulted in a rough surface morphology.

Another indicator of strain was the radius of curvature of the samples. By the end of the growth the curvatures reached 69km, 44km and 29km for samples 1–3, respectively. "The incorporation of BAlN can effectively minimize wafer warpage and alleviate tensile stress in AlN films," the team writes.

The final sample 1 with AlN buffer showed cracking effects (Figure 2). The BAlN buffer samples avoided cracking, but sample 3 had a rough surface.

The final surface roughness of sample 3 was 22.89nm, according to atomic force microscopy (AFM). The corresponding figures for the samples 1 and 2 were 0.45nm and 0.54nm.

Sample 2 combined the desirable features of no cracking and a smooth surface. The composition of the BAlN buffer in sample showed a B content around 4%, according to secondary-ion mass spectroscopy (SIMS). The buffer thickness was about 30nm, and the total thickness of the AlN/BAlN structure was around 520nm. Growth-rate monitoring during the MOCVD suggested that all the samples would have a similar total thickness.

The researchers comment: "Obviously, the actual B% in the buffer layer of sample 2 is significantly lower than the expected B/(B+Al) ratio of 20% introduced into the reactor. This discrepancy is attributed to the difficulty in incorporating B into the AlN layer."

AFM measurements on the buffer layers, showing an increase roughness of BAlN material, suggested that boron increases the nucleation site size from which crystal BAlN grows, first separately, and then coalesced into the desired AlN layer. Before coalescence, the islands increase roughness due to uneven growth rates and irregular merging.

The early coalescence in the sample 1 with only AlN as buffer accumulates stress into a too narrow region, creating the conditions for cracking.

Table 1. Material characterizations: densities (D) of screw and edge dislocations, and biaxial stress (σ).

Sample	D_{screw}	D_{edge}	σ
1	$1.76x10^9/cm^2$	$17.3x10^9/cm^2$	−2.67GPa
2	$1.04x10^9/cm^2$	$10.2x10^9/cm^2$	−1.63GPa
3	$6.50x10^9/cm^2$	$18.7x10^9/cm^2$	−1.30GPa

The researchers used x-ray analysis to derive the dislocation densities, and Raman spectroscopy for biaxial stress (Table b). The sample 2 with BAlN buffer showed reduced dislocation density and moderate tensile stress to avoid cracking, compared with the other samples. ■

https://doi.org/10.1063/5.0233425

Author: Mike Cooke

MESFETs on single crystal aluminium nitride substrate

Devices reach 2kV breakdown performance with short 15µm gate–drain distance.

Arizona State University (ASU) in the USA reports on high-voltage aluminium nitride (AlN) metal–semiconductor field-effect transistors (MESFETs) on single-crystal AlN substrates [Bingcheng Da et al, Appl. Phys. Express, v17, p104002, 2024]. The researchers claim their work as the first report of "AlN transistors via homoepitaxial growth on native substrates".

The team comments: "The devices showed good saturation and pinch-off behavior with high maximum I_{ds}, g_m and on/off ratio compared with AlN-on-sapphire devices without complicated contact layers."

AlN has the highest breakdown electric field, 12MV/cm, compared with potential ultrawide-bandgap (UWG) competitors, such as gallium oxide and diamond, putting it in the frame for future high-voltage, high-power applications. The best average breakdown electric field of the ASU devices was an order of magnitude down on the maximum possible, at 1.25MV/cm. However, this was still a 25% improvement on other reported AlN transistors produced on hetero-structures on foreign substrates such as sapphire or silicon carbide (SiC).

The use of homo-epitaxial AlN-on-AlN substrate enables lower defect densities to be realized. This is one hurdle jumped in the race to achieve high-performance power devices. Other challenges include improving the doping effectiveness for low-resistance channels, and enhancing the conductivity through the (desired) ohmic source/drain electrode contact.

The researchers used AlN substrates with a 10^3/cm^2 dislocation density for the AlN MESFETs (Figure 1). The epitaxial structure was grown using metal-organic chemical vapor deposition (MOCVD) from trimethyl-aluminium (TMAl), ammonia (NH_3), and silane (SiH_4) precursors. The growth conditions were 1250°C temperature and 20Torr pressure. A gallium nitride cap layer was included in the growth to protect the AlN from atmospheric oxidation. The resulting material demonstrated a 0.4nm surface roughness, and dislocation density of order 10^4/cm^2.

The team comments: "Compared with heteroepitaxial AlN on sapphire, homoepitaxial AlN on single-crystal AlN substrates had three orders of magnitude lower dislocation density, which can improve AlN device performance."

The MESFET devices were fabricated using inductively coupled plasma reactive ion etch to a depth of 700nm into the AlN resistive buffer layer; deposition of annealed titanium/aluminium/nickel/gold ohmic contact source/drain (S/D) electrodes; and deposition of the nickel/gold gate.

The source–gate (sg) and gate lengths were both 2µm. The gate–drain (gd) length was varied (2–15µm) to study the trade-off between on-resistance and break-down voltage. A longer L_{gd} increases on-resistance (bad), but lowers the peak electric field, increasing the breakdown voltage (good).

Electrical characterization between room temperature (RT=298K) and 473K showed reduced contact resistivity (ρ_c) and sheet resistance (R_{sh}) at higher temperatures: 0.77Ω-cm^2 and 2.4x10^{7}Ω/square at RT; and 0.15Ω-cm^2 and 6.6x10^{5}Ω/square at 473K, respectively.

The researchers comment: "The reduction in contact resistivity at high temperatures is likely due to easier passage of the thermally excited electrons through the metal/AlN interface by tunneling through an effective thinner potential barrier and/or thermionic emission."

The 2µm L_{gd} MESFETs demonstrated a normally-on

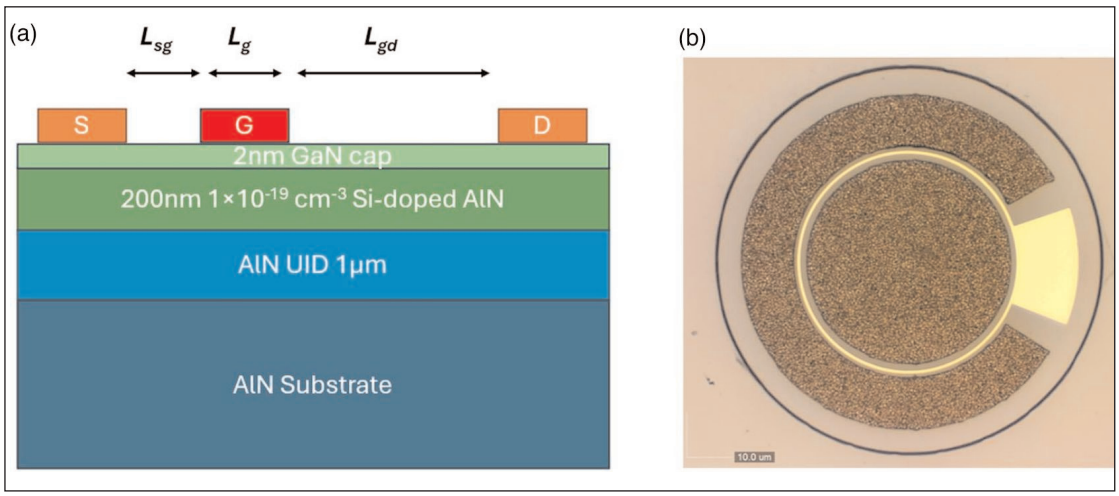

Figure 1. (a) Schematic cross-section and (b) top-view microscope image of fabricated AlN MESFET.

operation with a pinch-off at gate (V_{gs}) voltages less than –20V. For many applications a positive threshold, giving normally-off performance, is preferred, but AlN transistor development is presumably at too early a stage to think about that!

The maximum drain current (I_{ds}) at RT reached 56μA/mm at 9V V_{gs} — "6 times higher than that of the reported AlN-on-sapphire MESFETs," according to the team. The researchers go on to explain: "The increase in I_{ds} could be attributed to the lower sheet resistance of the homoepitaxial AlN layer ($2.4x10^7\Omega$/square) compared with that of AlN layers on sapphire ($8x10^7\Omega$/square)." The maximum transconductance reached 1.49μS/mm.

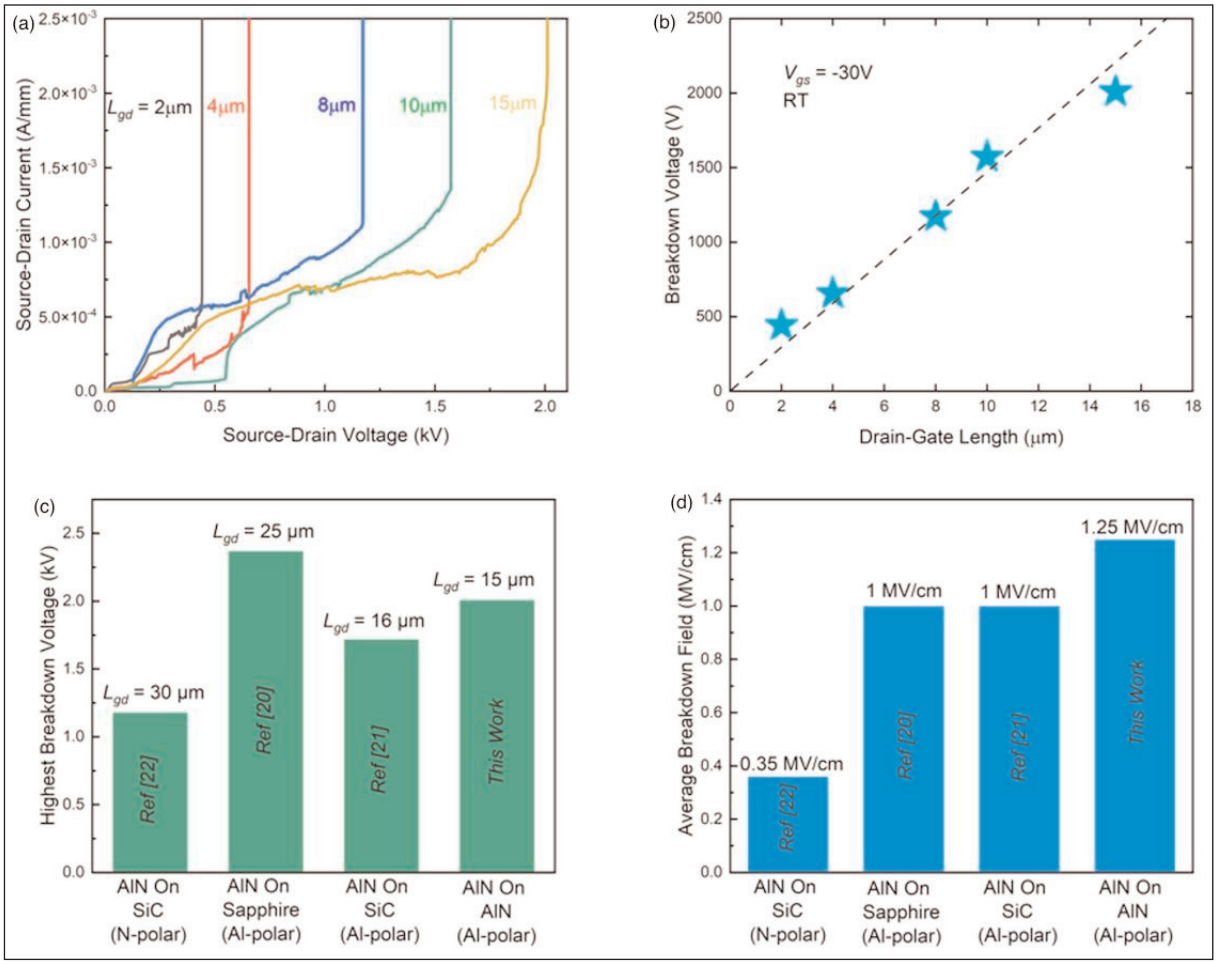

Figure 2. (a) Off-state breakdown characteristics with different L_{gd}. (b) Breakdown voltages versus L_{gd}. Comparison of reported AlN MESFETs in terms of (c) breakdown voltages and (d) average breakdown fields.

The devices with 8μm L_{gd} showed the lowest RT off current of $3.3x10^{-8}$A/mm, giving an on/off ratio of 700. While low compared to commercial transistors in other material systems, this value is around 6x higher than for previous AlN-on-sapphire MESFETs, the team says.

In experiments over the full 298–473K temperature range, the reverse gate leakage through the Schottky gate was less than $1.7x10^{-9}$A/mm at –20V V_{gd}. The researchers report: "Reverse gate leakage current was almost constant, showing stable gate control with increasing temperature."

The maximum drain current and transconductance increased between RT and 473K: from $2.06x10^{-5}$A/mm to $3.42x10^{-4}$A/mm; and from $1.19x10^{-6}$mS/mm to $2.45x10^{-5}$mS/mm, respectively.

The researchers explain: "There was a significant increase in the electron concentration from $1x10^{15}/cm^3$ to $5.6x10^{17}/cm^3$ as the temperature increased from RT to 500°C with a relatively small reduction in mobility from $156cm^2$/V-s to $52cm^2$/V-s. Consequently, the electrical conductance of the n-type AlN layer increased with rising temperature, leading to enhanced output performance at high temperatures. This is in contrast with conventional wide-bandgap semiconductors like GaN and SiC, where their overall forward performance of FETs based on these semiconductors deteriorates with increasing temperature due to a dominant reduction in electron mobility by phonon scattering."

Off-state breakdown at RT (Figure 2) occurred through destructive failure at the device edges. The researchers state that the breakdown came from electric field crowding effects. The gate potential was –30V. The longest 15μm L_{gd} device broke at 2010V, the second highest on a comparison chart, behind a 25μm L_{gd} transistor on sapphire, breaking at 2.3kV. However, the ASU structure enabled a 25% higher average electric field (1.25MV/cm) to be reached. The shorter L_{gd} of the ASU device allows a higher conductivity for target 2kV breakdown rating.

Looking ahead, the ASU teams reports: "Further work on implementing electric field management approaches such as field plates is underway to improve the breakdown field." ■

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Double-heterostructure gallium nitride for 5G FR2 mobile handsets

A GaN-on-silicon HEMT has achieved record saturated output power for low-voltage handset application.

Researchers based in Singapore claim a record saturated output power (P_{sat}) for gallium nitride (GaN) on silicon (Si) high-electron-mobility transistors (HEMTs) aimed at low-voltage (LV) high-frequency performance [Hanchao Li et al, IEEE Electron Device Letters, volume 45 (2024), issue 12 (December), p2315].

The team, from the National GaN Technology Centre (NGTC), the Institute of Microelectronics (IME), the Singapore–MIT Alliance for Research and Technology, and the National University of Singapore, comment on their double-heterostructure (DH) as opposed to conventional single-heterostructure (SH) device: "Till date, all the reported demonstrations are achieved using SH epitaxies, and the majority use deeply scaled gates (L_g<100nm). In comparison, the proposed transistor achieves excellent performance using a longer L_g of 120nm, and conventional ohmic and gate processes."

The researcher see great potential particularly for high transmit power in fifth-generation (5G) frequency range 2 (FR2) mobile handsets targeting high uplink/downlink rates (peak of 10/20gigabits/s). FR2 covers 24.25–71.0GHz, while FR1 is less than 7GHz. The gap 7–24.25GHz has been proposed, but not approved, as a 5G FR3. The GaN/Si HEMT option offers "the merits of GaN in power amplification with availability of wafers up to 300mm," according to the team.

The search for high-power, high-frequency performance tends to need shorter gate lengths, but such devices are negatively impacted by a range of "short-channel effects" (SCEs) that downgrade expectations of improved frequency performance from transistor scaling models.

The DH structure consisted of a GaN channel surrounded by aluminium nitride (AlN) top and AlGaN bottom barriers. SH devices just have the top barrier confining carriers to the channel.

The researchers comment on the DH HEMT structure: "Previous work has studied this heterostructure for higher-voltage power amplification. However, to the best of the authors' knowledge, the potential of DH HEMTs in low-voltage power amplification remains unexplored."

The double-heterostructure HEMT material was grown on high-resistivity silicon (HR-Si), using metal-organic chemical vapor deposition (Figure 1). The structure included an in-situ silicon nitride (SiN) layer to reduce gate leakage through the thin AlN barrier layer. The buffer was 1µm thick.

The AlGaN back barrier had an Al content of 8%. The back barrier was designed to increase carrier confinement in the channel region of the device, as suggested by 1D Schrodinger–Poisson band-structure calculations. The sheet carrier density was $1.7x10^{13}/cm^2$ and the mobility was $1400cm^2/V\text{-}s$, according to Hall measurements. The sheet resistance was 260Ω/square.

Device fabrication started with the source/drain contacts consisting of titanium/aluminium/nickel/gold, followed by plasma mesa etching for isolation. The T-gates consisted of nickel/gold. The HEMT was completed by a thin 10nm atomic layer deposition layer of aluminium oxide (Al_2O_3) as passivation.

The researchers comment: "The thin ALD-Al_2O_3 passivation layers could reduce the parasitic capacitance, while avoiding plasma-induced damage associated with PECVD processes, thereby offering more effective protection to the device's access region."

Previous work has studied this heterostructure for higher-voltage power amplification... The potential of DH HEMTs in low-voltage power amplification remains unexplored.

The thin ALD-Al_2O_3 passivation layers could reduce the parasitic capacitance, while avoiding plasma-induced damage associated with PECVD

The dimensions of the tested device included 120nm gate-length, 690nm spacings between the centrally placed gate from the source and drain contacts, and 2x16µm gate width. The relatively small width was designed to avoid self-heating effects, allowing better assessment of

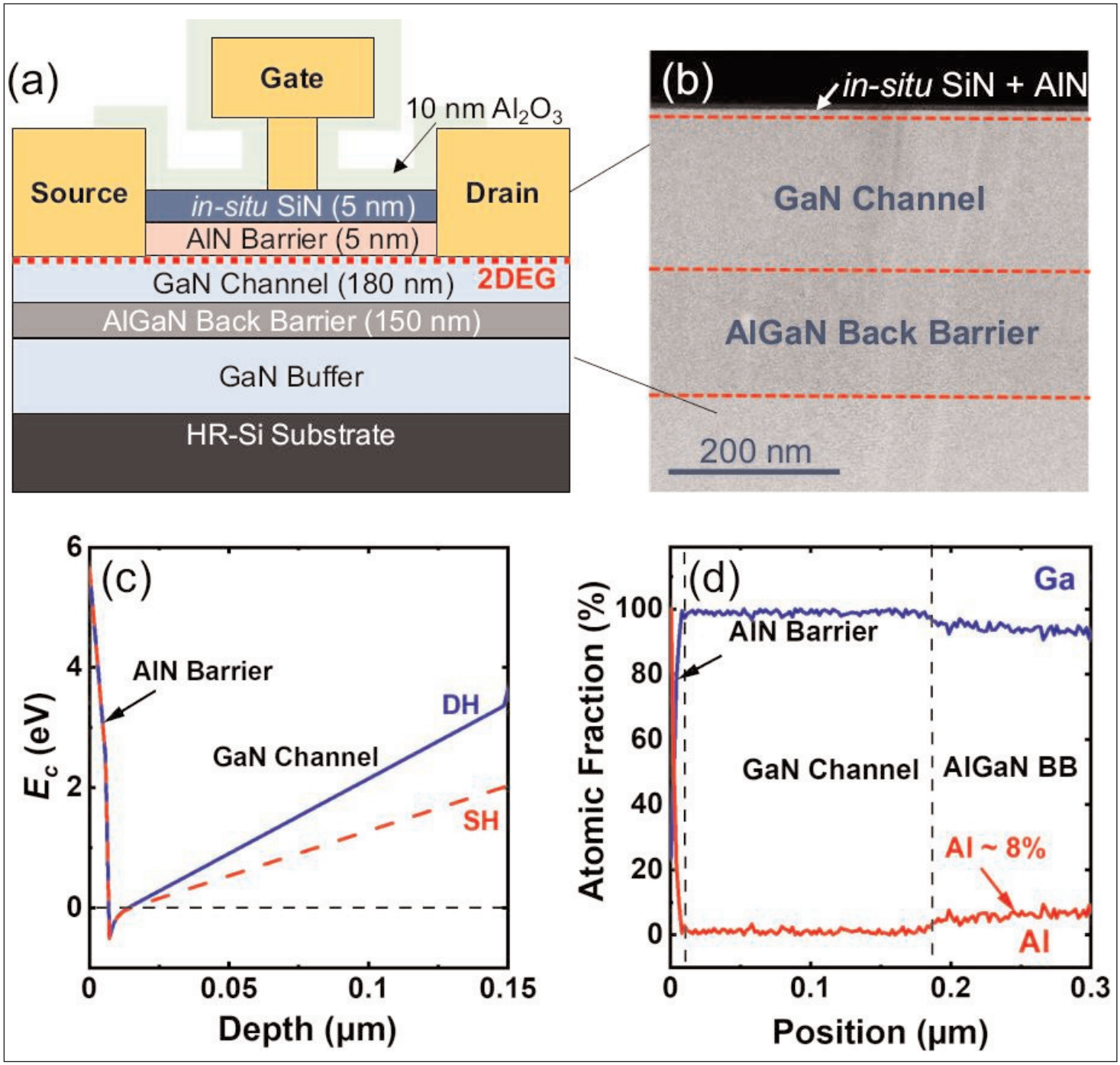

Figure 1. (a) Schematic cross-section of AlN/GaN/AlGaN DH HEMT. (b) Scanning transmission electron microscope (STEM) image of heterostructure. (c) Band diagrams of DH versus conventional SH hetero-structures. (d) Elemental composition of heterostructure from energy-dispersive x-ray spectroscopy (EDX).

the intrinsic performance of the DH transistor design.

The maximum drain current was 1.9A/mm with an ON-resistance of 1.5Ω-mm, and peak transconductance of 0.66S/mm. The threshold was negative (−2.9V), indicating normally-on/depletion-mode operation. The three-terminal breakdown voltage was 49V, giving an estimated breakdown electric field of 0.327MV/cm.

The researchers comment: "The breakdown mechanism is attributed to source–drain punch-through, which benefits from the design of the floating gate structure and the high quality of in-situ SiN."

The small-signal frequency performance measurements resulted in 145GHz cut-off (f_T) and 195GHz maximum oscillation (f_{max}) frequencies at 5V bias (V_d) and −2.5V gate potential (V_g). The f_T/f_{max} values were in the respective ranges 140–150/190–200GHz for biasing above 3V. The frequency–gate-length products were considered high at 17.4GHz-μm and 23.4GHz-μm for the cut-off and maximum oscillation, respectively. Multiplying the cut-off product by 2π gave a rough estimate for the carrier saturation velocity of $1.1x10^7$cm/s.

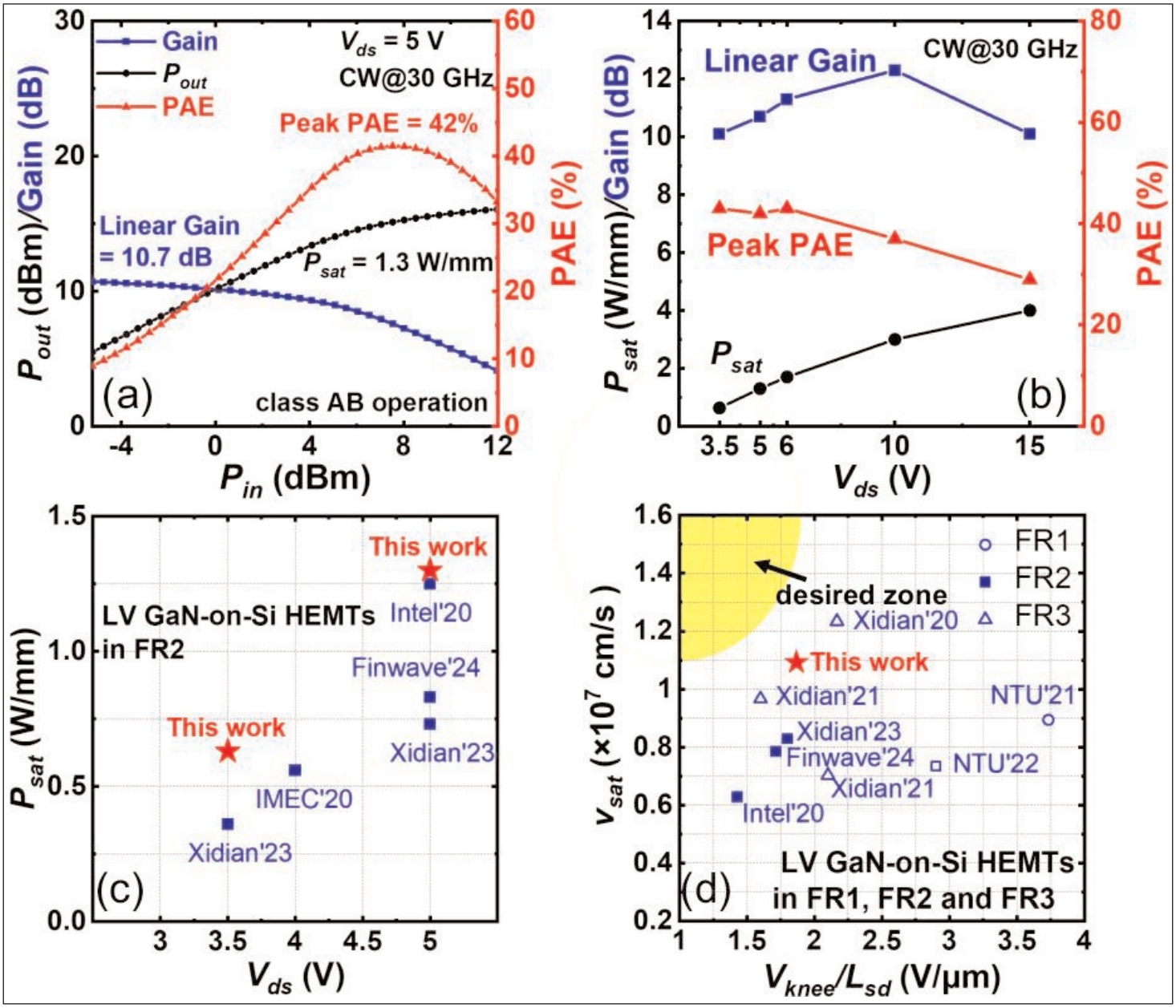

Figure 2. (a) Power sweep. (b) Load-pull performance versus Vds. (c) Benchmark of Psat versus V_{ds} for LV 5G FR2 operation. (d) Comparison of vsat versus Vknee (normalized by source/drain separation) for reported low-voltage GaN-on-Si transistors in FR1, FR2 and FR3.

The large-signal power capability (Figure 2) was assessed using on-wafer load-pull measurements at 30GHz fundamental frequency continuous wave (CW). The saturated output power (P_{sat}) was 1.3W/mm with 32% power-added efficiency (PAE) and 3.7dB gain. The peak PAE was 42% with an output power (P_{out}) of 1.1W/mm and 7.3dB gain.

The researchers see room for improvement in optimizing the passivation, more aggressive scaling, and ohmic contact design… Achieving a positive threshold voltage, and hence normally-off/enhancement-mode operation, would be beneficial for handset deployment

Reducing the bias to 3.5V enabled a slightly higher peak PAE of 43% with 0.52W/mm P_{out} and 7.2dB gain.

The P_{sat} value increased at an approximate linear rate up to 15V bias, reaching 4.0W/mm. The researchers comment: "The peak PAE decreased, mostly due to increased effect of traps and limited available load impedance tuning results of non-optimal matching condition."

The researchers see room for improvement in optimizing the passivation, more aggressive scaling, and ohmic contact design. They also suggest that achieving a positive threshold voltage, and hence normally-off/enhancement-mode operation, would be beneficial for handset deployment. ■

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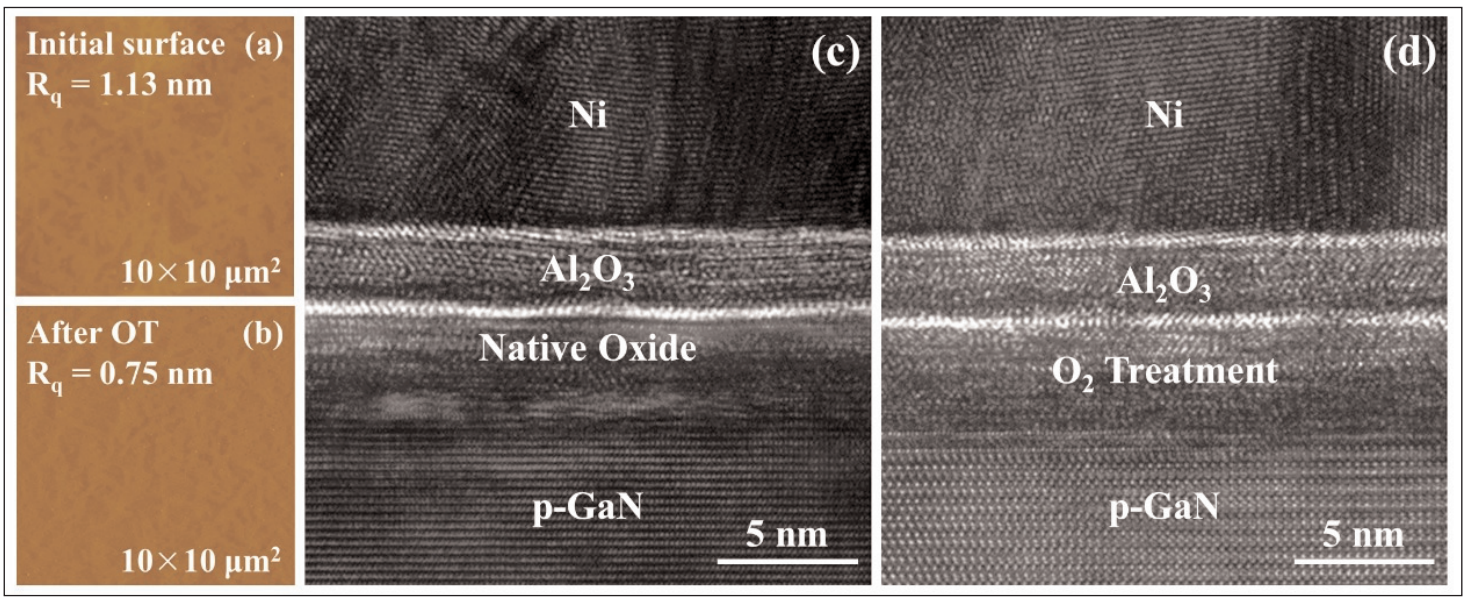
High-breakdown-voltage P-GaN gate HEMTs with threshold voltage of 7.1V

Thermal oxidation treatment of P-GaN combined with atomic layer deposition prior to gate metal deposition

Shandong University has reported an enhancement-mode P-GaN/AlGaN/GaN metal-insulator-semiconductor high-electron-mobility transistors (MIS-HEMTs) by combining thermal oxidation treatment of P-GaN with atomic layer deposition (OTALD) prior to gate metal deposition [Siheng Chen et al, IEEE Electron Device Letters, vol. 45, no. 12, pp2343–2346, December 2024, doi: 10.1109/LED.2024.3478819]. Compared with traditional devices, the device presented increased threshold voltage significantly from 1.8V to 7.1V, with improved gate breakdown voltage and off-state breakdown voltage of 26.9V and 1980V, respectively.

When used as power devices, P-GaN/AlGaN/GaN HEMTs require high threshold voltage, high gate voltage swing, high breakdown voltage and low gate leakage current. A low activation rate of magnesium (Mg) dopants in P-GaN typically results in a threshold voltage of less than 2V without additional processing, limiting the application of P-GaN/AlGaN/GaN HEMTs in high-gate-voltage drive circuits. Therefore, improving the threshold voltage is a pressing challenge. In response to this issue, the researchers applied a combination of oxygen annealing treatment (OT) of P-GaN and atomic layer deposition (ALD) technology, achieving the highest threshold voltage on record with high gate breakdown voltage and high off-state breakdown voltage. This research demonstrates the immense potential of OTALD technology in power electronic devices requiring high gate drive voltages, thereby expanding the possibilities for widespread application in P-GaN power devices.

The epitaxial structure in this study based on a Si (111) substrate consists of a 100nm P-GaN cap layer with an Mg doping concentration of $3x10^{19}cm^{-3,}$ a 12.5nm $Al_{0.18}Ga_{0.82}N$ barrier layer, a 0.5nm AlN spacer layer, a 450nm undoped GaN channel layer and a 4μm high-resistance GaN buffer layer that were grown by metal-organic chemical vapor deposition (MOCVD). Device fabrication commences with highly selective etching of the P-GaN cap layer, and mesa isolation of the device was completed subsequently by inductively coupled plasma (ICP) etching. The ohmic contacts were formed using a metal stack of Ti/Al/Ni/Au via magnetron sputtering and annealing in N_2 atmosphere. After depositing a SiO_2 passivation layer using plasma-enhanced chemical vapor deposition (PECVD), the opening of the gate region was patterned by ICP



Cross-sectional TEM image of the MIS contact of (c) ALD-HEMTs and (d) OTALD-HEMTs.

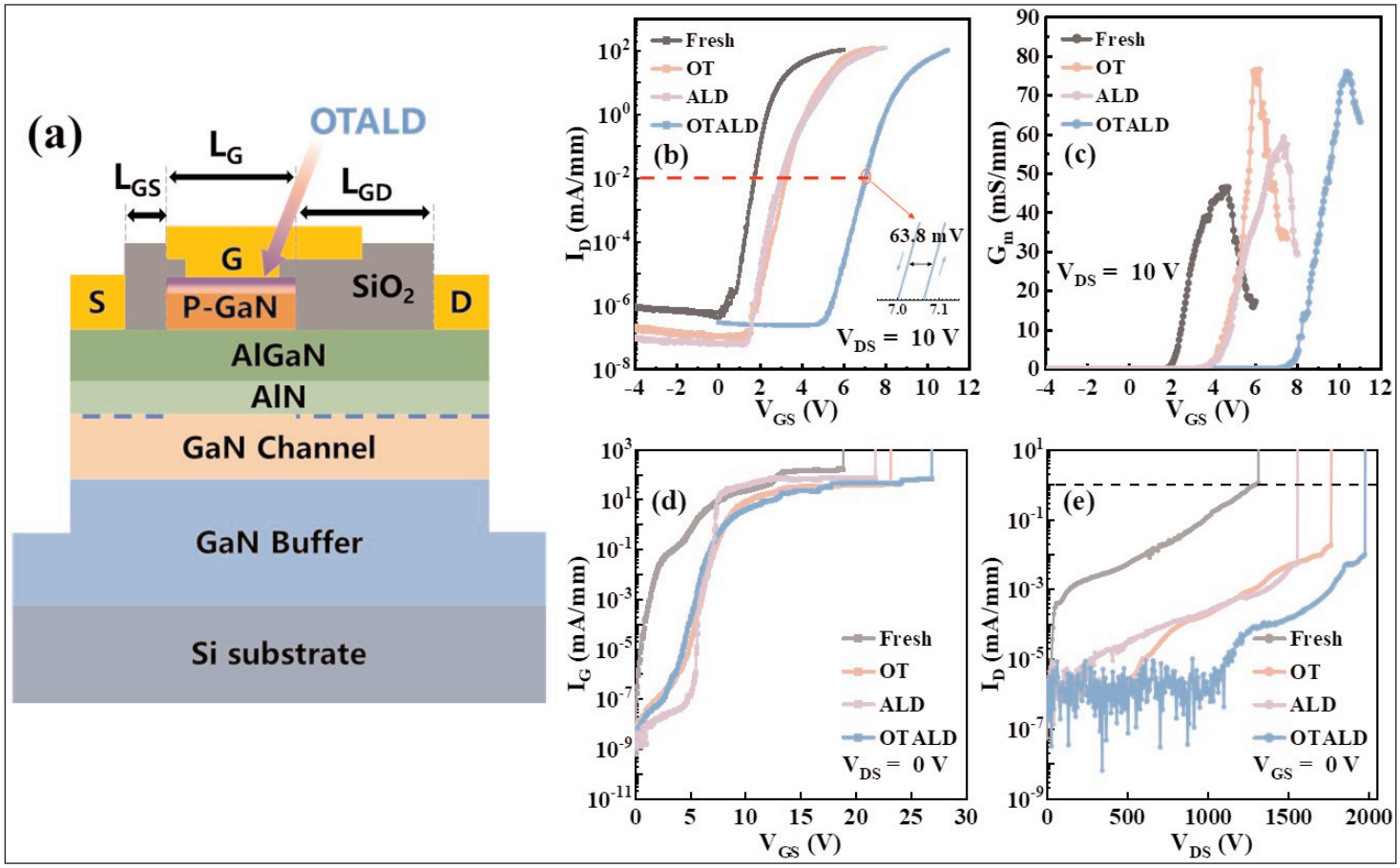


Figure 2: (a) Schematic cross section of OTALD-HEMTs. (b) Transfer and (c) transconductance characteristic of four types of P-GaN gate HEMTs. (d) Gate breakdown and (e) off-state breakdown characteristics of four types of P-GaN gate HEMTs.

etching. The fabrication of the MIS structure on the opening of the P-GaN gate region by OTALD technology started with the thermal oxidation treatment. This is to form a thin oxide layer by low-temperature annealing process in oxygen atmosphere. Followed by deposition of a 5nm Al_2O_3 dielectric layer by plasma-enhanced atomic layer deposition (PEALD) process. Finally, a Ni/Au gate metal stack was deposited by magnetron sputtering to form the gate metal field plate. The untreated fresh P-GaN gate HEMTs were fabricated as references. All devices have the same size with a P-GaN gate length (L_G) of 4μm, a gate–drain spacing (L_{GD}) of 12μm, a gate–source spacing (L_{GS}) of 4μm and a gate width (W_G) of 100μm. The length of the gate field-plate is 2μm.

Atomic force microscopy (AFM) measurement shows decreased surface roughness after the oxygen annealing treatment process, indicating that this process produces a flat oxide layer on the P-GaN surface and effectively removes other contaminants. Cross-sectional high-resolution transmission electron microscopy (HRTEM) shows that a dense and smooth oxide layer is formed. The presence of this oxide layer provides a gradually varied transition between Al_2O_3 and P-GaN, leading to a significantly improved interface quality between these two materials.

Owing to the higher gate Schottky barrier of the oxide layer and the voltage division effect of the dielectric layer, OTALD-HEMTs allow the threshold voltage to be increased significantly from 1.8V to 7.1V compared with conventional P-GaN gate HEMTs, with a minimal hysteresis of 63.8mV and high on/off current ratio above 10^8. The smooth interface of the oxide layer can reduce the scattering of the two-dimensional electron gas (2DEG) within the channel, contributing to a higher transconductance (75.9mS/mm, an increase of 63%) with a higher saturation output current density at V_{GS} = 11V. The dense oxide layer possesses a wider bandgap and higher thermodynamic stability than P-GaN, which is less susceptible to degradation caused by hot-electron bombardment and suppression of gate leakage current. Also, the presence of the dielectric layer beneath the gate can reduce surface states and fill defects on P-GaN surfaces, decreasing the leakage current and suppressing hot-carrier effects. Thus, the OTALD-HEMT further enhanced the forward gate breakdown and off-state breakdown voltage to 26.9V and 1980V, which are improvements of 42% and 51% respectively compared with the conventional P-GaN gate HEMT. The OTALD-HEMTs exhibit the high gate breakdown voltage, off-state breakdown voltage as well as record highest threshold voltage among previously reported P-GaN

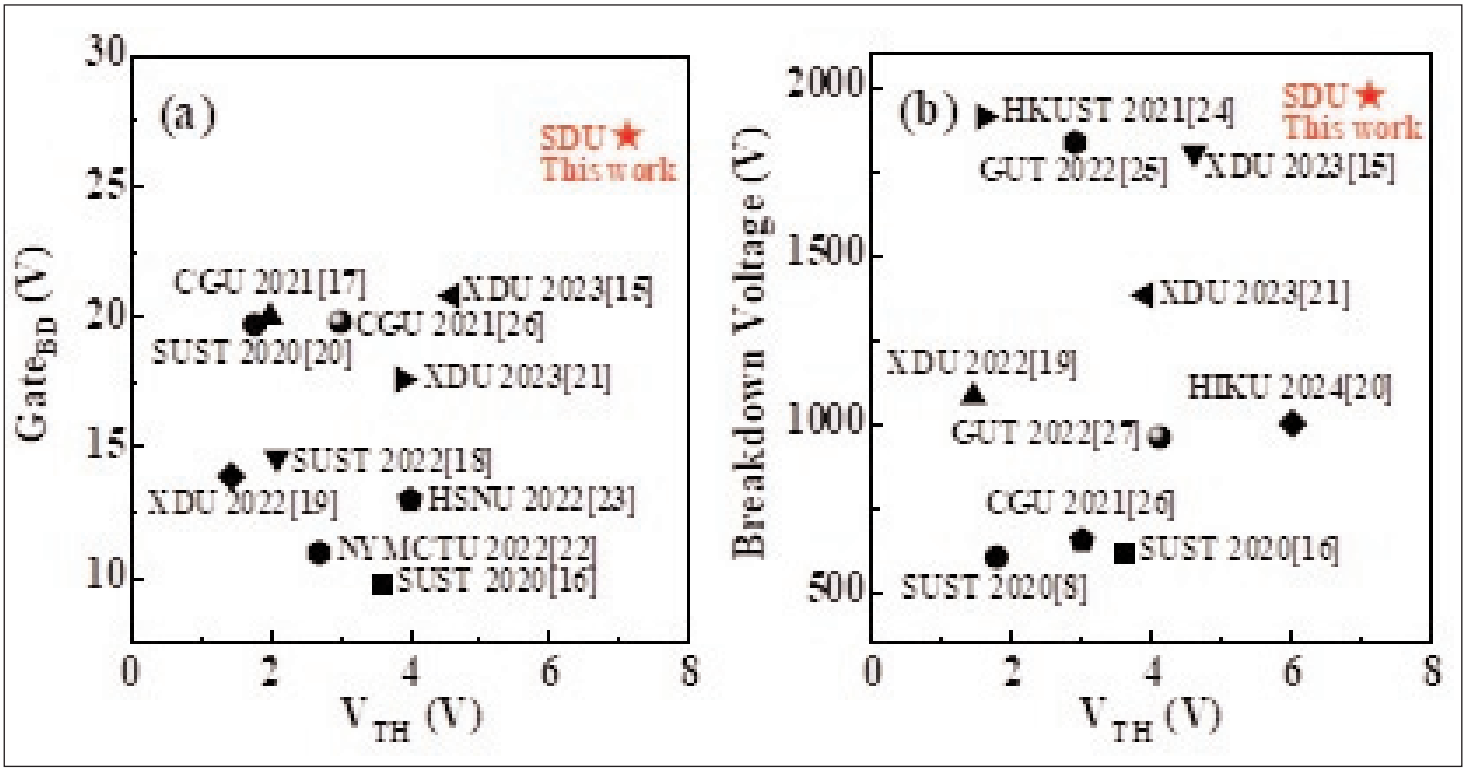


Figure 3: Comparison for (a) gate breakdown and (b) off-state breakdown with different threshold voltage between this work and other studies.

gate devices, indicating that OTALD technology holds substantial potential for enhancing VT_H and further improving device performance.■

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Vital Thin Film Materials (Guangdong) Co Ltd (Vital Materials subsidiary)
18G, 18th Floor, Shenzhen Free
Trade Centre, No.111 Taizi Road,
Nanshan District,
Shenzhen, Guangdong, China 518067
Tel: (+86) 0755-21651348
sales@vitaltfm.com

www.vitaltfm.com
Vital Materials is the world's leading producer of rare metals as well as the first Chinese manufacturer to deliver G11 rotary ITO target. Vital is also one of the world's three major supplier of infrared materials, a key supplier of compound semiconductor substrates, and a strategic partner of the world's largest thin film solar manufacturer.

6 Deposition equipment

AIXTRON SE
Dornkaulstr. 2,
52134 Herzogenrath,
Germany
Tel: +49 2407 9030 0
Fax: +49 2407 9030 40
www.aixtron.com

ETC (LPE subsidiary)
Via Falzarego, 820021 Baranzate (Mi),
Italy
Tel: +39 02 383 41 51
Fax: +39 02 383 06 118
www.lpe-epi.com

Evatec AG
Hauptstrasse 1a,
CH-9477 Trübbach,
Switzerland
Tel: +41 81 403 8000
Fax: +41 81 403 8001
www.evatecnet.com

FHR Anlagenbau Gmbh
(Vital Materials subsidiary)
Am Hügel 2, D-01458
Ottendorf-Okrilla,
Germany
Tel: +49 35205 520-0
E-mail: sales@fhr.de
E-mail: sales@vitalchem.com
www.fhr.biz
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LPE S.p.A.
Via Falzarego, 8
20021 Baranzate (Mi), Italy
Tel: +39 02 383 41 51
Fax: +39 02 383 06 118
www.lpe-epi.com

PLANSEE High Performance Materials
6600 Reutte,
Austria
Tel: +43 5672 600 2422
info@plansee.com
www.plansee.com

Plasma-Therm LLC
10050 16th Street North,
St. Petersburg, FL 33716,
USA
Tel: +1 727 577 4999
Fax: +1 727 577 7035
www.plasmatherm.com

Riber
31 rue Casimir Périer, BP 70083,
95873 Bezons Cedex,
France
Tel: +33 (0) 1 39 96 65 00
Fax: +33 (0) 1 39 47 45 62
www.riber.com

SVT Associates Inc
7620 Executive Drive,
Eden Prairie, MN 55344,
USA
Tel: +1 952 934 2100
Fax: +1 952 934 2737
www.svta.com

Temescal, a division of Ferrotec
4569-C Las Positas Rd,
Livermore, CA 94551,
USA
Tel: +1 925 245 5817
Fax: +1 925 449-4096
www.temescal.net

Veeco Instruments Inc
100 Sunnyside Blvd.,
Woodbury, NY 11797,
USA
Tel: +1 516 677 0200
Fax: +1 516 714 1231
www.veeco.com

7 Wafer processing materials

Kayaku Advanced Materials Inc
200 Flanders Road,
Westborough, MA 01581,
USA
Tel: +1 617 965 5511
www.kayakuam.com

Praxair Electronics
(see section 5 for full contact details)

Versum Materials
8555 S. River Parkway,
Tempe, AZ 85284,
USA
Tel: +1 602 282 1000
www.versummaterials.com

8 Wafer processing equipment

Evatec AG
Hauptstrasse 1a,
CH-9477 Trübbach,
Switzerland
Tel: +41 81 403 8000
Fax: +41 81 403 8001
www.evatecnet.com

EV Group
DI Erich Thallner Strasse 1,
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Fax: +43 7712 5311 4600
www.EVGroup.com
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Tel: +44 (0) 1389 875 444
Fax: +44 (0) 1389 879 042
www.logitech.uk.com

Plasma-Therm LLC
(see section 6 for full contact details)

SAMCO International Inc
532 Weddell Drive,
Sunnyvale, CA, USA
Tel: +1 408 734 0459
Fax: +1 408 734 0961
www.samcointl.com

SPTS Technology Ltd
Ringland Way, Newport NP18 2TA,
Wales, UK
Tel: +44 (0)1633 414000
Fax: +44 (0)1633 414141
www.spts.com

SUSS MicroTec AG
Schleißheimer Strasse 90,
85748 Garching, Germany
Tel: +49 89 32007 0
Fax: +49 89 32007 162
www.suss.com

Synova SA
Ch. de la Dent d'Oche,
1024 Ecublens,
Switzerland
Tel +41 21 694 35 00
Fax +41 21 694 35 01
www.synova.ch

TECDIA Inc
2700 Augustine Drive, Suite 110,
Santa Clara, CA 95054 ,
USA
Tel: +1-408-748-0100
Fax: +1-408-748-0111
Contact Person: Cathy W. Hung
Email: sales@tecdia.com
www.tecdia.com

Veeco Instruments Inc
(see section 6 for full contact details)

9 Materials & metals

Goodfellow Cambridge Ltd
Ermine Business Park, Huntingdon,
Cambridgeshire PE29 6WR, UK
Tel: +44 (0) 1480 424800
Fax: +44 (0) 1480 424900
www.goodfellow.com

PLANSEE High Performance Materials
6600 Reutte,
Austria
Tel: +43 5672 600 2422
info@plansee.com
www.plansee.com

TECDIA Inc
2700 Augustine Drive, Suite 110,
Santa Clara, CA 95054,
USA
Tel: +1 408 748 0100
Fax: +1 408 748 0111
www.tecdia.com

10 Gas and liquid handling equipment

Cambridge Fluid Systems
12 Trafalgar Way, Bar Hill,
Cambridge CB3 8SQ,
UK
Tel: +44 (0)1954 786800
Fax: +44 (0)1954 786818
www.cambridge-fluid.com

CS CLEAN SOLUTIONS GmbH
Fraunhoferstrasse 4,
Ismaning, 85737,
Germany
Tel: +49 89 96 24000
Fax: +49 89 96 2400122
www.csclean.com

Entegris Inc
129 Concord Road,
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Fax: +1 978 436 6735
www.entegris.com

IEM Technologies Ltd
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Fax: +44 (0)1278 420666
www.iemtec.com

Vacuum Barrier Corporation
4 Barton Lane,
Woburn, MA 01801,
USA
Tel: +1 781 933 3570
Fax: +1 781 933 9428
www.vacuumbarrier.com

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Versum Materials
8555 S. River Parkway,
Tempe, AZ 85284, USA
Tel: +1 602 282 1000
www.versummaterials.com

11 Process monitoring and control

Conax Technologies
2300 Walden Avenue,
Buffalo, NY 14225,
USA
Tel: +1 800 223 2389
Tel: +1 716 684 4500
www.conaxtechnologies.com

k-Space Associates Inc
2182 Bishop Circle
East, Dexter, MI 48130,
USA
Tel: +1 734 426 7977
Fax: +1 734 426 7955
www.k-space.com

KLA-Tencor
One Technology Dr,
1-2221I, Milpitas,
CA 95035, USA
Tel: +1 408 875 3000
Fax: +1 408 875 4144
www.kla-tencor.com

LayTec AG
Seesener Str. 10–13,
10709 Berlin,
Germany
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Fax: +49 30 89 00 180
www.laytec.de

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Fax: +1 781 933 9428
www.vacuumbarrier.com

VACUUM BARRIER VBC CORPORATION

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WEP (Ingenieurbüro Wolff für Elektronik- und Programmentwicklungen)
Bregstrasse 90,
D-78120 Furtwangen im Schwarzwald,
Germany
Tel: +49 7723 9197 0
Fax: +49 7723 9197 22
www.wepcontrol.com

12 Inspection equipment

Bruker
Oestliche Rheinbrueckenstrasse 49,
Karlsruhe, 76187, Germany
Tel: +49 (0)721 595 2888
Fax: +49 (0)721 595 4587
www.bruker.com

KLA–Tencor
160 Rio Robles, Suite 103D,
San Jose, CA 94538-7306,
USA
Tel: +1 408 875-3000
Fax: +1 510 456-2498
www.kla-tencor.com

13 Characterization equipment

J.A. Woollam Co. Inc.
645 M Street Suite 102,
Lincoln, NE 68508, USA
Tel: +1 402 477 7501
Fax: +1 402 477 8214
www.jawoollam.com

Lake Shore Cryotronics Inc
575 McCorkle Boulevard,
Westerville, OH 43082, USA
Tel: +1 614 891 2244
Fax: +1 614 818 1600
www.lakeshore.com

14 Chip test equipment

Riff Company Inc
1484 Highland Avenue, Cheshire,
CT 06410, USA
Tel: +1 203-272-4899
Fax: +1 203-250-7389
www.riff-co.com

Tektronix Inc
14150 SW Karl Braun Drive,
P.O.Box 500, OR 97077, USA
www.tek.com

15 Assembly/packaging materials

ePAK International Inc
4926 Spicewood Springs Road,
Austin, TX 78759, USA
Tel: +1 512 231 8083
Fax: +1 512 231 8183
www.epak.com

Gel-Pak
31398 Huntwood Avenue,
Hayward, CA 94544, USA
Tel: +1 510 576 2220
Fax: +1 510 576 2282
www.gelpak.com

Wafer World Inc
(see section 3 for full contact details)

Materion Advanced Materials Group
2978 Main Street,
Buffalo, NY 14214, USA
Tel: +1 716 837 1000
Fax: +1 716 833 2926
www.williams-adv.com

16 Assembly/packaging equipment

CST Global Ltd
4 Stanley Boulevard,
Hamilton International
Technology Park,
Blantyre, Glasgow G72 0BN, UK
Tel: +44 (0) 1698 722072
www.cstglobal.uk

Kulicke & Soffa Industries
1005 Virginia Drive,
Fort Washington,
PA 19034,
USA
Tel: +1 215 784 6000
Fax: +1 215 784 6001
www.kns.com

Palomar Technologies Inc
2728 Loker Avenue West,
Carlsbad, CA 92010,
USA
Tel: +1 760 931 3600
Fax: +1 760 931 5191
www.PalomarTechnologies.com

PI (Physik Instrumente) L.P.
16 Albert St . Auburn ,
MA 01501, USA
Tel: +1 508-832-3456,
Fax: +1 508-832-0506
www.pi.ws
www.pi-usa.us

TECDIA Inc
2700 Augustine Drive, Suite 110,
Santa Clara, CA 95054,
USA
Tel: +1 408 748 0100
Fax: +1 408 748 0111
www.tecdia.com

17 Assembly/packaging foundry

Quik-Pak
10987 Via Frontera,
San Diego, CA 92127, USA
Tel: +1 858 674 4676
Fax: +1 8586 74 4681
www.quikicpak.com

18 Chip foundry

CST Global Ltd
4 Stanley Boulevard, Hamilton International Technology Park,
Blantyre, Glasgow, G72 0BN,
UK
Tel: +44 (0) 1698 722072
www.cstglobal.uk

United Monolithic Semiconductors
Route departementale 128,
BP46, Orsay, 91401,
France
Tel: +33 1 69 33 04 72
Fax: +33 169 33 02 92
www.ums-gaas.com

19 Facility equipment

RENA Technologies NA
3838 Western Way NE,
Albany, OR 97321, USA
Tel: +1 541 917 3626
www.rena-na.com

Vacuum Barrier Corporation
4 Barton Lane, Woburn, MA 01801,
USA
Tel: +1 781 933 3570
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www.vacuumbarrier.com

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20 Facility consumables

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Austria
Tel: +43 5672 600 2422
info@plansee.com
www.plansee.com

W.L. Gore & Associates
401 Airport Rd, Elkton,
MD 21921-4236,
USA
Tel: +1 410 392 4440
Fax: +1 410 506 8749
www.gore.com

21 Computer hardware & software

Crosslight Software Inc
121-3989 Henning Dr.,
Burnaby, BC, V5C 6P8,
Canada
Tel: +1 604 320 1704
Fax: +1 604 320 1734
www.crosslight.com

Semiconductor Technology Research Inc
10404 Patterson Ave.,
Suite 108, Richmond,
VA 23238,
USA
Tel: +1 804 740 8314
Fax: +1 804 740 3814
www.semitech.us

22 Used equipment

Brumley South Inc
422 North Broad Street,
Mooresville,
NC 28115,
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www.ClassOneEquipment.com

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Fax: +1 203-250-7389
www.riff-co.com

TECDIA Inc
2700 Augustine Drive, Suite 110,
Santa Clara,
CA 95054 ,
USA
Tel: +1-408-748-0100
Fax: +1-408-748-0111
Contact Person: Cathy W. Hung
www.tecdia.com

24 Resources

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7140 San Jose, CA 95126, USA
Tel: +1 408 289 9555
www.alshuktz.com

SEMI Global Headquarters
San Jose, CA 95134,
USA
Tel: +1 408 943 6900
www.semi.org

Yole Développement
69006 Lyon,
France
Tel: +33 472 83 01 86
www.yole.fr

event calendar

If you would like your event listed in *Semiconductor Today*'s Event Calendar, then please e-mail all details to the Editor at mark@semiconductor-today.com

16–20 February 2025
2025 IEEE International Solid-State Circuits Conference (ISSCC)
San Francisco, CA, USA
E-mail: issccinfo@yesevents.com
www.isscc.org

19–21 February 2025
SEMICON Korea 2025
Korea World Trade Tower, Seoul, South Korea
E-mail: semiconkorea@semi.org
www.semiconkorea.org/en

26–28 February 2025
Asia Photonics Expo (APE 2025)
Level 1, Sands Expo & Convention Centre (Marina Bay Sands), Singapore
E-mail: visitors-ape@informa.com
www.asiaphotonicsexpo.com

2–6 March 2025
11th International Workshop on Semiconducting Oxides (IWSC-2025)
Arizona State University, Tempe, Arizona, USA
E-mail: Farida.Selim@asu.edu
https://semte.engineering,asu.edu/semiconductor-workshop

16–20 March 2025
IEEE Applied Power Electronics Conference (APEC 2025)
Atlanta, GA, USA
E-mail: apec@apec-conf.org
www.apec-conf.org

26–28 March 2025
SEMICON China 2025
Shanghai New International Expo Centre (SNIEC), Shanghai, China
E-mail: semichina@semi.org
www.semiconchina.org

30 March – 3 April 2025
Optical Fiber Communication Conference and Exhibition (OFC 2025)
Moscone Convention Center, San Francisco, CA, USA
E-mail: custserv@optica.org
www.ofcconference.org

1 April 2025
ITF Photonics USA 2025 - Shedding light on advances in integrated photonics
W Hotel, San Francisco, CA, USA
www.imecitf.com/photonics

29 April – 1 May 2025
28th Annual Components for Military & Space Electronics Conference & Exhibition (CSME 2025)
Four Points by Sheraton (LAX), Los Angeles, CA, USA
E-mail: info@tjgreenllc.com
www.tjgreenllc.com/cmse

4–8 May 2025
LightFair 2025
Las Vegas Convention Center, Las Vegas, NV, USA
E-mail: info@lightfair.com
www.lightfair.com

advertisers' index

4–9 May 2025
2025 Conference on Lasers & Electro-Optics (CLEO)
Long Beach, CA, USA
E-mail: info@cleoconference.org
www.cleoconference.org

6–8 May 2025
PCIM 2025: Expo & Conference on Power Electronics, Intelligent Motion, Renewable Energy and Energy Management
Nuremberg, Germany
E-mail: pcim_visitors@mesago.com
www.mesago.de/en/PCIM/main.htm

27–30 May 2025
2025 IEEE 75th Electronic Components and Technology Conference (ECTC)
Gaylord Texan Resort & Convention Center, Dallas, TX, USA
www.ectc.net

8–12 June 2025
2025 Symposium on VLSI Technology & Circuits – 'Cultivating the VLSI Garden: From Seeds of Innovation to Thriving Growth'
Rihga Royal Hotel, Kyoto, Japan
www.vlsisymposium.org

22–25 June 2025
83rd annual Device Research Conference (DRC)
Duke University, Durham, NC, USA
E-mail: sud70@psu.edu
https://2025.deviceresearchconference.org

15–17 June 2025
IEEE Radio Frequency Integrated Circuits Symposium (RFIC 2025)
San Francisco, CA, USA
E-mail: support@mtt.org
www.rfic-ieee.org

15–20 June 2025
2025 IEEE/MTT-S International Microwave Symposium (IMS 2025)
San Francisco, CA, USA
E-mail: exhibits@horizonhouse.com
www.ims-ieee.org/about-ims/past-and-future-ims

22–27 June 2025
World of PHOTONICS CONGRESS — International Congress on Photonics in Europe
ICM — International Congress Center, Messe München, Munich, Germany
E-mail: info@photonics-congress.com
www.photonics-congress.com/en

6–11 July 2025
15th International Conference on Nitride Semiconductors (ICNS-15)
Malmö, Sweden
E-mail: info@icns15.com
https://mkon.nu/icns-15

22–25 July 2025
ALD/ALE 2025: AVS 25th International Conference on Atomic Layer Deposition (ALD 2025) featuring the 12th International Atomic Layer Etching Workshop (ALE 2025)
Jeju Island, South Korea
E-mail: della@avs.org
www.ald2025.avs.org

29–31 July 2025
7th International Congress on Advanced Materials Sciences and Engineering 2025 (AMSE-2025) — "Transforming Technologies for a Sustainable Future"
Krakow, Poland
E-mail: eve@istci.org
https://istci.org/amse2025/Register.asp

10–12 September 2025
China International Optoelectronic Exposition (CIOE 2025)
Shenzhen World Exhibition and Convention Center, Shenzhen, Guangdong, China
E-mail: cioe@cioe.cn
www.cioe.cn/en

21–26 September 2025
28th European Microwave Week (EuMW 2025)
Jaarbeurs, Utrecht, the Netherlands
E-mail: eumwreg@itnint.com
www.eumweek.com

24–26 September 2025
PCIM Asia – International Exhibition and Conference for Power Electronics, Intelligent Motion, Renewable Energy and Energy Management (PCIM Asia Shanghai 2025)
Shanghai New International Expo Centre, China
E-mail:pcimasia@china.messefrankfurt.com
www.pcimasia-expo.com

28 September – 2 October 2025
ECOC 2025: 51st European Conference on Optical Communication
Bella Center, Copenhagen, Denmark
E-mail:ecoc2025@cap-partner.eu
www.ecoc2025.org

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